80286–BASED PRODUCTS

TECHNICAL REFERENCE GUIDE – VOLUME I

COMPAQ®

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Volume I

CONTENTS

NOTATIONAL CONVENTIONS

Values

I/O addresses and other values are in hexadecimal notation when shown with the letter h after them. Memory addresses are always in hexadecimal and are expressed as SSSS:0000, where SSSS is a 16-bit segment and 0000 is a 16-bit offset. All other numbers are in decimal notation.

Ranges

Ranges or limits for a parameter are shown as a pair of values separated by two dots (..). For example, 4..0 includes numbers 4, 0, and every number in between (3, 2, and 1).

Signal Labels

Signal values are labelled A0, A1, A15, etc. Signal names are in upper case. Signal names with a dash (-) as a suffix indicate that that signal is negative when true, or active when low.

Bit values are labelled bit 7, bit 6, bit 0, etc.

Labels with the smallest suffixes (A0, bit 0) have the least significance or value.

Register Notation and Usage

The standard Intel naming conventions are used for the 80286 registers. AX, BX, CX, and DX are the names of the general registers when used as word-length registers (16-bit). AH, AL, BH, BL, CH, CL, DH, and DL are the names for the general registers when they are used as byte-length registers (8-bit). When addresses are handled, BX usually contains the offset. However, SI (source index) or BP (base pointer) may also be used with the ES register.

The ES register denotes the extra segment and is used exclusively for address-segment parameter passing; FL is the flag register used to return the status of some operations. Status is given as the state of one of the flags within the register: CF for carry flag, IF for interrupt flag, etc.

The shaded register-set boxes are ignored on input and are unchanged for output. An exception is that the contents of AX are not guaranteed to be preserved across all calls. Always reload the function code in AH and the parameter in AL (if any) to repeat a call. Register contents are always preserved across BIOS calls, unless the register is used to return a value.

Bit Notation

Bit fields within a byte or word are shown as a range of decimal numbers separated by two dots <..> and enclosed in angle brackets. For example, reference to the four most-significant bits in a word is made with <15..12>. The higher number, representing the most-significant bit, is on the left.

Common Abbreviations

The following abbreviations are used throughout this guide:

Abbr.	Meaning	Comment
CNTLR	Controller	
DMA	Direct Memory Access	
FRI	Flux Reversals per Inch	
INT	Interrupt	
KB	Kilobyte	1024 Bytes
MB	Megabyte	1,024,000 Bytes
ms	Millisecond	Always preceded by a number
ns	Nanosecond	Always preceded by a number
RAM	Random-Access Memory	
ROM	Read-Only Memory	
RTC	Real-Time Clock	
TPI	Tracks Per Inch	
us	Microsecond	Always preceded by a number

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4,499,531
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4,499,531
4,574,279

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80286-Based Products Technical Reference Guide

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Compaq Computer Corporation

PREFACE

This manual provides hardware and firmware (ROM) information for the COMPAQ PORTABLE 286 and COMPAQ DESKPRO 286 Personal Computers for:

- People who want to know more about the hardware in their system and general theories about how the system works.
- Technicians or engineers who need technical information to design accessories for the system.
- Programmers who need to know about the hardware (programmable devices) and firmware (ROM) for programming purposes.

HOW TO USE THIS DOCUMENT

The most important features of any computer system are:

- What kind of processor does it have?
- How much memory can it support?
- How fast is it?
- What can be added to it?

Chapter 1 introduces the COMPAQ PORTABLE 286 and COMPAQ DESKPRO 286 Personal Computers, with answers to all these questions. Everyone should read Chapter 1 first.

Chapter 2 describes the system boards for both the COMPAQ PORTABLE 286 and COMPAQ DESKPRO 286 Personal Computers.

Chapters 3 through 13 describe the system components in detail.

Chapter 14 is a BIOS Programming Guide that explains the system firmware.

Appendix A lists the system error messages.

Appendix B describes the COMPAQ Asynchronous Communication/Parallel Printer Board.

The index will help you quickly find the information you need.

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COMPAQ DESKPRO 286 SYSTEM MEMORY BOARD

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Chapter 1
SYSTEM OVERVIEW

1.1 INTRODUCTION

Chapter 1 introduces the COMPAQ PORTABLE 286® and COMPAQ DESKPRO 286® Personal Computers. It also includes information relating to the entire system, such as:

- System characteristics
- System components
- System specifications
- System interconnection
- Introduction to the Intel 80286 Microprocessor, including the system memory map and I/O map
- System features
- Connectors

The COMPAQ PORTABLE 286 and COMPAQ DESKPRO 286 Personal Computer systems are advanced general-purpose computers. Both systems have the same high performance capabilities. The main difference between them is the portability feature of the COMPAQ PORTABLE 286.

The COMPAQ DESKPRO 286 has greater memory expansion, more board slots, larger fixed disk drive storage capability, requires an external monitor, and can operate at 6, 8, or 12 MHz, depending on the version of the system board installed.

Figures 1-1 and 1-2 show the two systems.

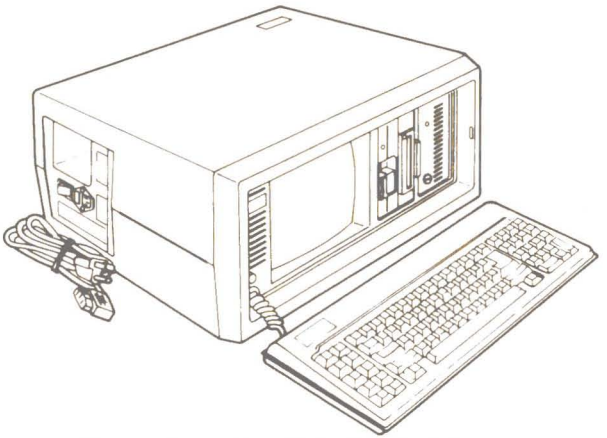

Figure 1-1. COMPAQ PORTABLE 286

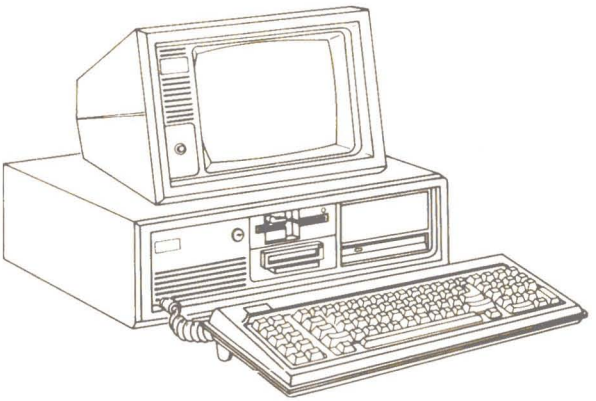

Figure 1-2. COMPAQ DESKPRO 286

1.2 SYSTEM CHARACTERISTICS

The COMPAQ PORTABLE 286 and COMPAQ DESKPRO 286 Personal Computers have the following characteristics:

- The 80286 microprocessor with a 8-MHz variable processing speed.

NOTE: The COMPAQ Portable 286 and the 8-MHz COMPAQ DESKPRO 286 have data processing speeds which are switchable between 8-MHz and 6-Mhz. The 12-MHz COMPAQ DESKPRO 286 has a switchable processing speed of 12-MHz and 8-MHz.

- Up to 2.7 Megabytes (COMPAQ PORTABLE 286) or 8.1 Megabytes (COMPAQ DESKPRO 286) of physical memory (using COMPAQ memory option boards).
- Numerous mass data storage options, including:
  - Diskette drives (360 Kbyte or 1.2 Megabyte)
  - Fixed disk drives (20, 30, 40, or 70 Megabyte). (20-Megabyte fixed disk drive is the only size available for the COMPAQ PORTABLE 286.)
  - 10-Megabyte fixed disk drive backup (tape) (COMPAQ PORTABLE 286 and 8-MHz COMPAQ DEKSPRO 286) and
  - 40-Megabyte fixed disk drive backup (tape) (8-MHz and 12-MHz COMPAQ DESKPRO 286).
- Software compatibility with most popular programs written for the IBM PC AT.
- For the COMPAQ DESKPRO 286, a choice of two keyboards: The 101-key (U.S.)/102-key (international) COMPAQ Enhanced Keyboard or the 84-key keyboard. The COMPAQ PORTABLE 286 uses the 84-key keyboard.

NOTE: If your COMPAQ DESKPRO 286 Personal Computer is equipped to operate at 12 MHz, the 101-key (U.S. English)/102-key (international) COMPAQ Enhanced Keyboard is the only available keyboard.

- Asynchronous communications (serial) and printer (parallel) interfaces.
- Choice of two video display controller boards: either the COMPAQ Video Display Controller Board for graphics and high-resolution text or the Color Graphics board for high-resolution graphics.
- Real-time clock with battery backup.
- Security lock.
- Multipurpose controller board.
- Multipurpose fixed disk controller board (COMPAQ DESKPRO 286, 12 Mhz only).

Table 1-1 lists features of the standard models of the COMPAQ PORTABLE 286 Personal Computers that operate at 8 and 6 MHz.

Table 1-2 lists features of the 8 MHz and 12 Mhz COMPAQ DESKPRO 286 personal computers.

Table 1-1. Features of the COMPAQ PORTABLE 286 Personal Computers

	COMPAQ PORTABLE 286	
Features	Model 1	Model 2
80287 Coprocessor	Socket	Socket
Base memory size	256 KB	640 KB
Memory expansion without adding board	640 KB	640 KB
Maximum memory with (#) expansion boards	2.7 MB(1)	2.7 MB(1)
360-KB diskette drive	Option	Option
1.2-megabyte diskette drive	Standard	Standard
10-megabyte fixed disk drive backup (tape)	Option	Option
40-megabyte fixed disk drive backup (tape)	Option	Option
20-megabyte fixed disk drive (3.5 inch)	Option	Standard
Asynchronous interface (9 pin)	Standard	Standard
(Printer) interface	Standard	Standard
Security lock	Standard	Standard
Available expansion slots	3	2
Total expansion slots	5	5

Table 1-2. Features of the Various Models of 8 MHz and 12 MHz COMPAQ DESKPRO 286 Personal Computers

	COMPAQ DESKPRO 286	
Features	8 MHz	12 MHz
80287 Coprocessor Socket	Socket (6 MHz)	Socket (8MHz)
Maximum Base memory size	640 KB	640 KB
Memory expansion without adding board	2.1 MB	2.1 MB
Maximum memory with (#) expansion boards	8.1 MB(3)	8.1 MB(3)
360-KB diskette drive	Supported	Supported
1.2-megabyte diskette drive	Standard	Standard
10-megabyte fixed disk drive backup (tape)	Supported	
40-megabyte fixed disk drive backup (tape)	Supported	Supported
30-megabyte fixed disk drive	Supported	
70-megabyte fixed disk drive	Supported	Supported
20-megabyte intergrated fixed disk drive	Supported	
40-megabyte intergrated fixed disk drive	Supported (Note)	Supported
Asynchronous interface (9 pin)	Standard	Standard
Printer interface	Standard	Standard
Security lock	Standard	Standard
Expansion slots	8	8

Note: Requires a multipurpose fixed disk controller board.

1.3 SYSTEM COMPONENTS FOR 80286-BASED COMPAQ PERSONAL COMPUTERS OPERATING AT 8 AND 6 MHZ

The 8-MHz and 6-MHz COMPAQ PORTABLE 286 and COMPAQ DESKPRO 286 Personal Computers are general-purpose computers with the following major components:

- System boards with:
  - An Intel 80286 microprocessor
  - A socket for an 80287 coprocessor
  - Expansion slots for mass data storage devices, video display controller boards, communication ports, and other hardware options
  - Programmable devices, such as DMA circuits, a keyboard controller, an interval timer, and an interrupt controller

The functions of the system boards for the two computers are similar, but the ROM and RAM for the COMPAQ DESKPRO 286 System Board Version 1 are on a separate memory board.

- A multipurpose controller board that supports two internal diskette drives and one fixed disk drive backup. The asynchronous communications and printer interfaces provide for communications with parallel or serial printers, modems, and other devices.
- A dual-mode video display controller board that supports the COMPAQ Dual-Mode Monitor and compatible monochrome and color (RGBI) monitors. (Optional with the COMPAQ DESKPRO 286) (Internal color monitors are not available for the COMPAQ PORTABLE 286.)
- An optional COMPAQ Color Monitor and COMPAQ Enhanced Color Graphics Board are available. (See the COMPAQ Enhanced Color Graphics Board Guide for details.)
- Mass data storage devices, such as diskette drives, fixed disk drives, and fixed disk drive backup systems, depending on the model.
- A power supply that provides the required voltages and current for the system board, keyboard, and typical expansion boards, such as video controllers and memory expansion boards.
- A fixed disk drive controller board that supports selected fixed disk drive options.

Figure 1-3 shows the system functional block diagram, which is the same for both systems, operating at 8 and 6 MHz.

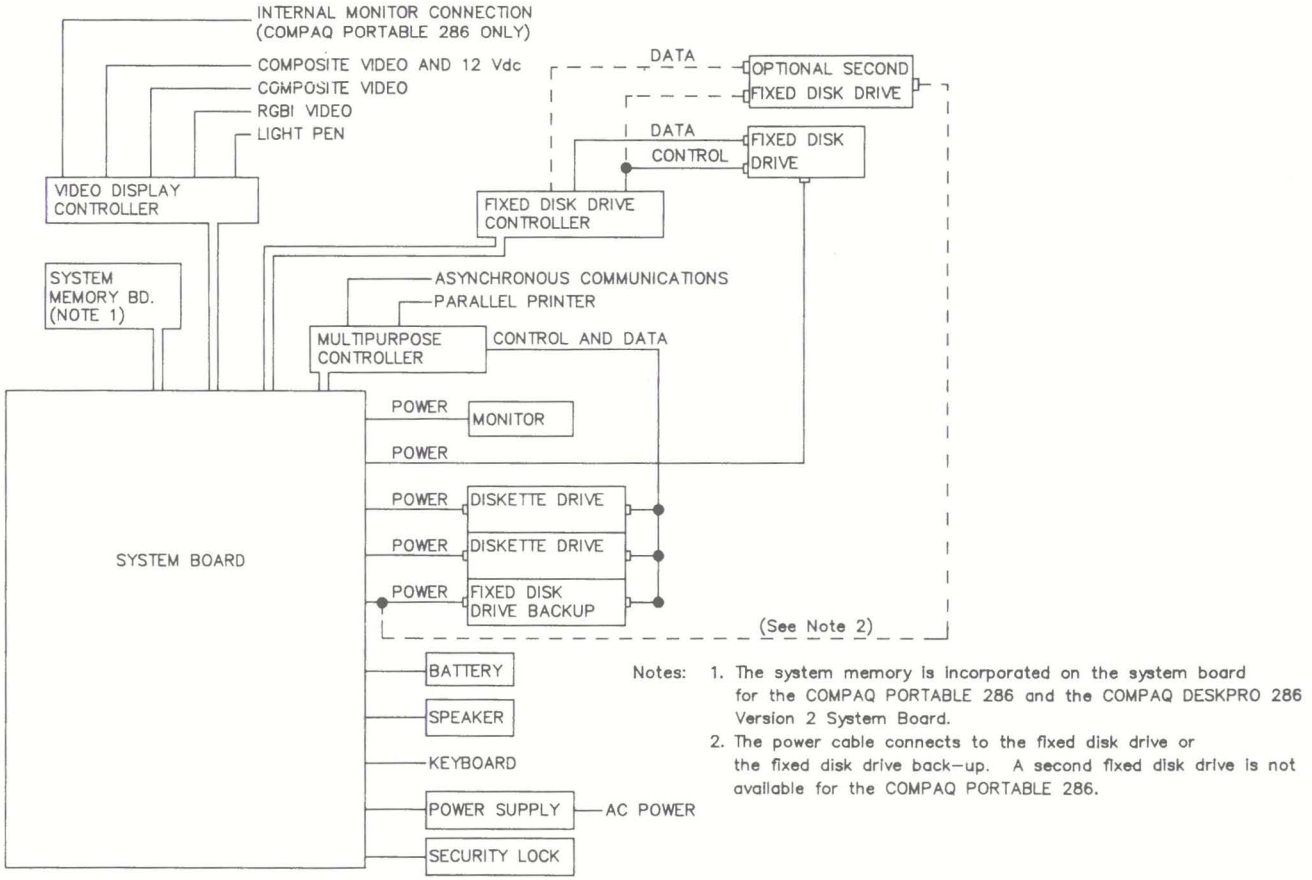

Figure 1-3. System Block Diagram for Both Systems (COMPAQ Portable 286 and COMPAQ DESKPRO 286) Operating at 8 and 6 MHz

1.4 SYSTEM COMPONENTS FOR 80286-BASED COMPAQ PERSONAL COMPUTERS OPERATING AT 12 AND 8 MHZ

The COMPAQ DESKPRO 286 Personal Computer, equipped to operate at 12 MHz, has the following major components:

- System boards with:
  - A 12-MHz 80286 microprocessor
  - A socket for an 8-MHz 80287 coprocessor
  - Expansion slots for mass data storage devices, video display controller boards, communications ports, and other hardware options.
  - Programmable devices, such as direct memory access (DMA) circuits, a keyboard controller, an interval timer, and an interrupt controller.
- A multipurpose fixed disk controller board that supports two internal diskette drives, a maximum of two fixed disk drives with integrated controllers and one fixed disk drive backup. The asynchronous communications and printer interfaces provide for communications with parallel or serial printers, modems, and other devices.
- An optional dual-mode video display controller board that supports COMPAQ Dual-Mode Monitor, COMPAQ Color Monitor and compatible monochrome and color (RGBI) monitors.
- An optional COMPAQ Color Monitor and COMPAQ Enhanced Color Graphics Board are available. (See the COMPAQ Enhanced Color Graphics Board Guide for details.)
- Mass data storage devices, such as diskette drives, fixed disk drives, and fixed disk drive backup systems, depending on the model.
- A power supply that provides the required voltages and current for the system board, keyboard, and typical expansion boards.
- A fixed disk drive controller board that supports selected fixed disk drive options.

Figure 1-4 shows the system functional block diagram for the 12-MHz COMPAQ DESKPRO 286 Personal Computer.

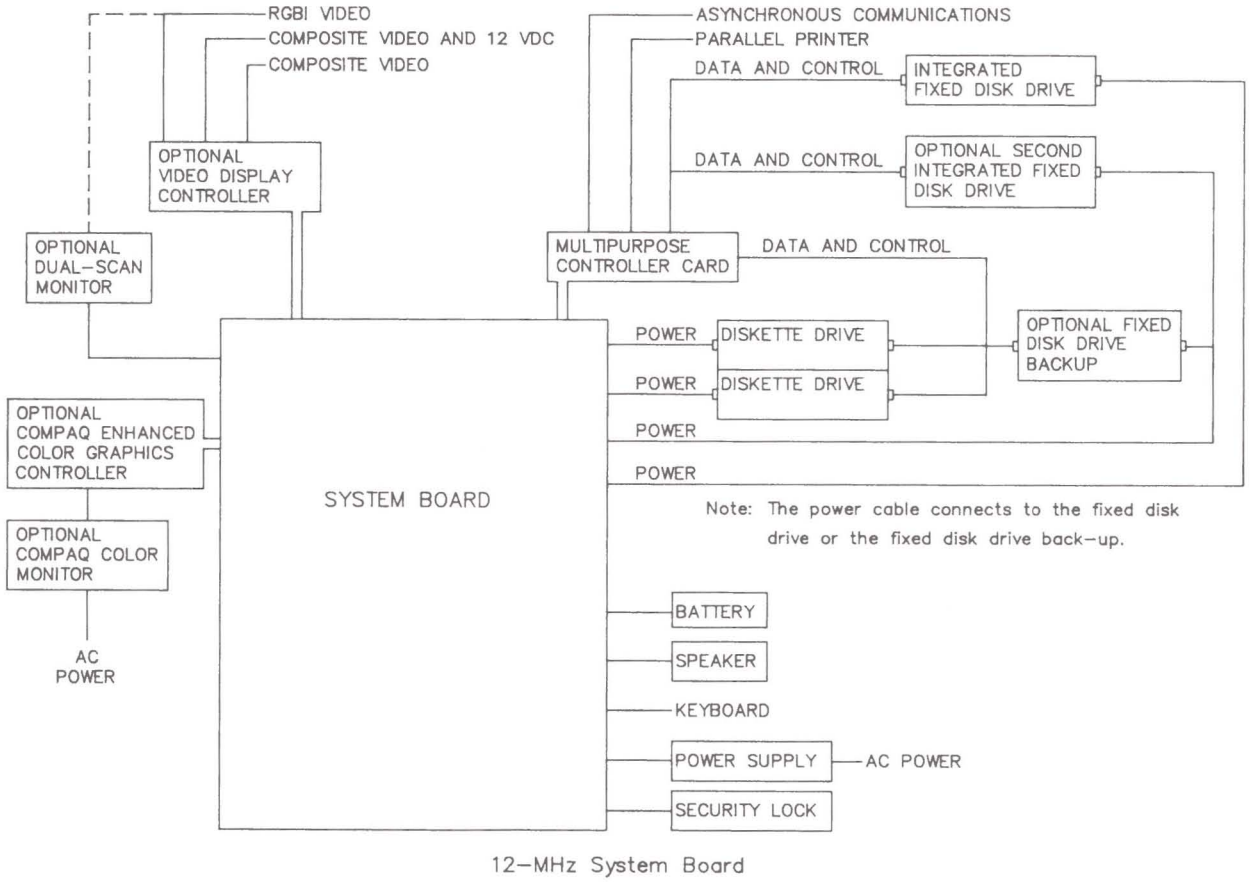

Figure 1-4. System Block Diagram for the 12-MHz COMPAQ DESKPRO 286 Personal Computer

1.5 SYSTEM SPECIFICATIONS

Tables 1-3 and 1-4 list the system specifications for the COMPAQ PORTABLE 286 and the COMPAQ DESKPRO 286 Personal Computers.

Table 1-3. COMPAQ PORTABLE 286 System Specifications

System size:	Width 20.0 in (508 mm) Height 8.5 in (216 mm) Depth 16.0 in (406 mm)
Weight:	Model 1: 30.3 lb (13.7 kg); Model 2: 33 lb (15.0 kg)
Air temperature:	Operating 50° to 104°F (10 to 40°C) Nonoperating 50° to 140°F (10 to 60°C) Shipping -22° to 140°F (-30 to 60°C)
Relative humidity (noncondensing):	Nonoperating 5% to 90% Operating 20% to 80%
Heat output:	Varies according to options installed; 1024 BTU/hr (maximum)
Noise level (acoustical):	Varies according to options installed. Nominal sound power levels (A Scale) in decibles per ANSI S1.29-1979 are: 54 (without Fixed Disk Drive Backup) 59 (with Fixed Disk Drive Backup)
Shock (Ref. Mil-Std-810C):	The values, in G's for 11 ms half-sine, of the levels of shock that the system can withstand with no damage are: Operating: 5 Nonoperating: 30
Vibration:	Values, in G's, 0 to peak, sinusoidal, 5 to 500 Hz, 1/2 octave per minute, of the levels of vibration that the system can withstand with no damage are: Operating: 0.25 Nonoperating: 0.50
AC power required (47 to 62 Hz):	120 VAC, nominal, with range of 102 to 132 VAC RMS, 3 A maximum, or 230 VAC, nominal, with range of 204 to 264 VAC RMS, 2.5 A maximum
Maximum altitude:	Operating 10,000 ft (3 000 m) Shipping 30,000 ft (9 000 m)
Agency compliances:	See Chapter 13 for additional monitor specifications. 120 VAC: UL478; CSA22.2; FCC Part 15, Class B 220-240 VAC: IEC380; DIN IEC 380/VDE 806; VDE 871, Class B

Table 1-4. COMPAQ DESKPRO 286 System Specifications

System size:	Width 19.8 in (503 mm) Height 6.4 in (162 mm) Depth 16.5 in (419 mm)
Weight:	Model 1: 37 lb (16.8 kg); Model 20: 42.4 lb (19.1 kg); Model 40: 44 lb (20.0 kg)
Air temperature:	Operating 50° to 104°F (10° to 40°C) Nonoperating 50° to 140°F (10° to 60°C) Shipping -22° to 140°F (-30° to 60°C)
Relative humidity (noncondensing):	Nonoperating 5%to 90% Operating 20%to 80%
Heat output:	Varies according to options installed 1229 BTU/hr (maximum)
Noise level (acoustical):	Varies according to options installed. Nominal sound power levels (A Scale) in decibles per ANSI S1.29-1979 are: 53 (without Fixed Disk Drive Backup) 62 (with Fixed Disk Drive Backup)
Shock (Ref. Mil-Std-810C):	The values, in G's for 11 ms half-sine, of the levels of shock that the system can withstand with no damage are: Operating: 5 Nonoperating: 20
Vibration:	Values, in G's, 0 to peak, sinusoidal, 5 to 500 Hz, 1/2 octave per minute, of the levels of vibration that the system can withstand with no damage are: Operating: 0.5 Nonoperating: 0.75
AC power required (47 to 62 Hz):	120 VAC, nominal, with range of 102 to 132 VAC RMS, 4 A max. (5 A max., 12 MHz Deskpro 286) or 230 VAC, nominal, with range of 204 to 264 VAC RMS, 2.5 A max. (4 A max., 12 MHz Deskpro 286)
Maximum altitude:	Operating 10,000 ft (3 000 m) Shipping 30,000 ft (9 000 m)
Agency compliances:	See Chapter 13 for additional monitor specifications. 120 VAC: UL478; CSA22.2; FCC Part 15, Class B 220-240 VAC: IEC380; DIN IEC 380/VDE 806; VDE 871, Class B

1.6 SYSTEM INTERCONNECTIONS

This section shows interconnections diagrams for the following types of COMPAQ personal computers:

- COMPAQ PORTABLE 286 Personal Computer
- COMPAQ DESKPRO 286 Personal Computer (8-MHz)
- COMPAQ DESKPRO 286 Personal Computer (12-MHz)

Figure 1-5 shows the interconnection diagram for the COMPAQ PORTABLE 286.

Figure 1-6 shows the interconnection diagram for the 8-MHz COMPAQ DESKPRO 286 Personal Computer.

Figure 1-7 shows the interconnection diagram for the 12-MHz COMPAQ DESKPRO 286 Personal Computer.

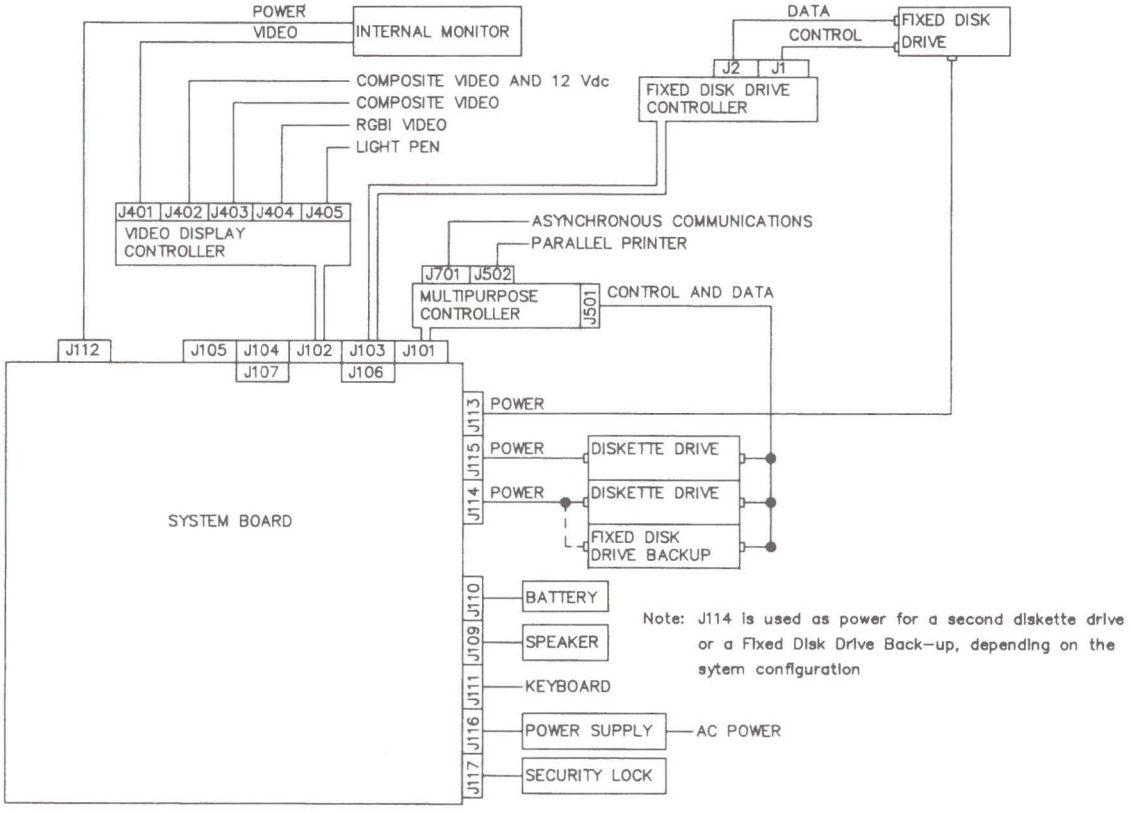

Figure 1-5. COMPAQ PORTABLE 286 Interconnection Diagram

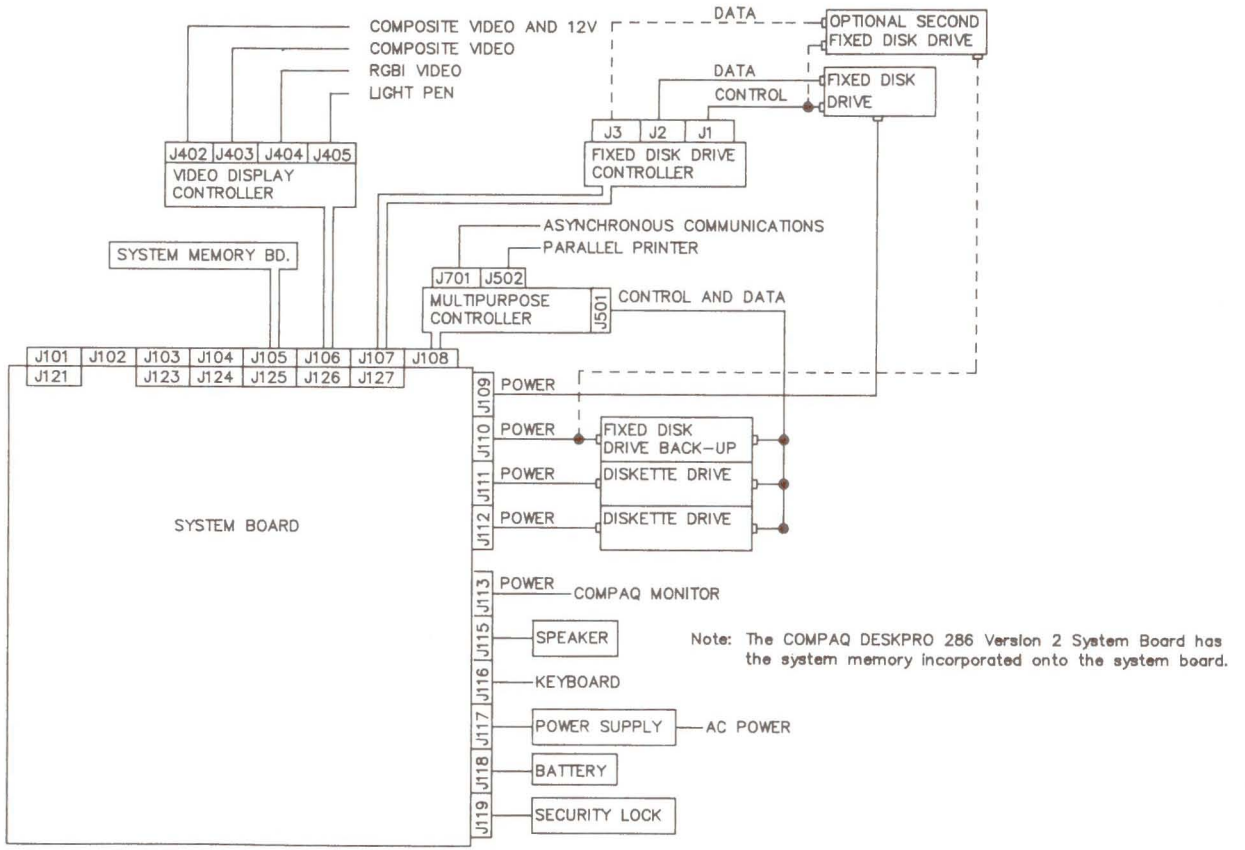

Figure 1-6. COMPAQ DESKPRO 286 (8-MHz) Interconnection Diagram

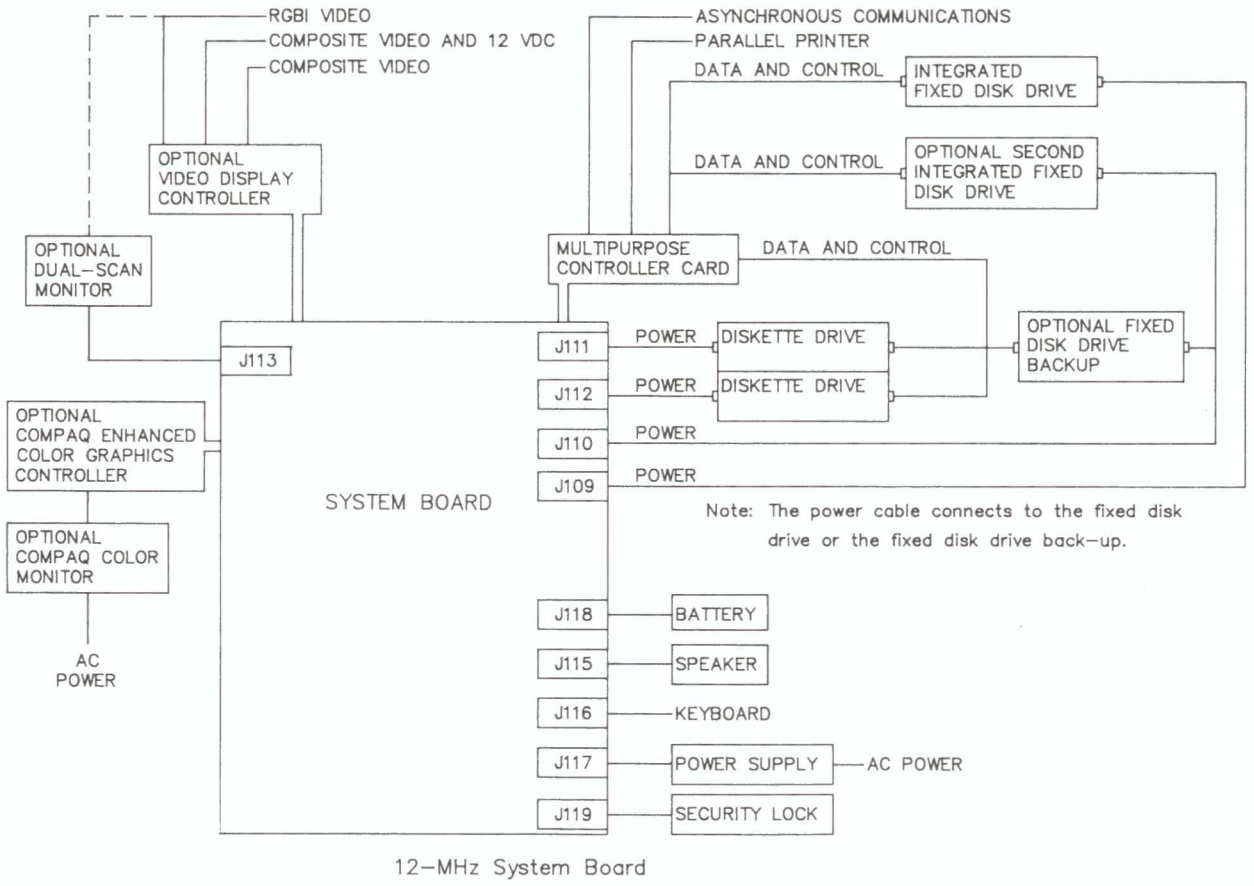

Figure 1-7. COMPAQ DESKPRO 286 (12-MHz) Interconnection Diagram

1.7 INTRODUCTION TO THE INTEL 80286 MICROPROCESSOR

The Intel 80286 is a 16-bit microprocessor. It is not only compatible with the Intel 8088 and 8086 processors, but has other enhancements, such as greater speed, multitasking and multiuser capabilities, and an on-chip virtual-memory management unit.

80286 Software Concepts

The 80286 has two modes of operation: the Real mode and the Protected mode.

Real Mode

In the Real mode, the 80286 operates with the same memory limitations as the 8086 processor. That is, the 80286 addresses 1 Megabyte of memory using only the 20 least-significant bits of the 24-bit address bus.

Protected Mode

In Protected mode, the 80286 operates in a virtual-memory environment. It uses the full 24-bit address bus to directly address as many as 16 megabytes of real memory. In the virtual-memory environment, programs can specify 1 billion memory locations (1 gigabyte).

A disk operating system capable of virtual-memory operation transfers data in blocks so that a specified 30-bit virtual-memory location is addressed within the 24-bit real memory space. An operating system capable of managing the Protected mode must be loaded into the system to use this mode.

80286 Hardware Concepts

The 80286 is a 68-pin very-large-scale-integrated (VLSI) circuit that serves as the central processor.

The 80286 uses three buses; a 24-bit address bus, a 16-bit data bus, and a control bus to communicate with and control the rest of the system.

All devices outside the 80286 are addressed as either memory-mapped devices or I/O-mapped devices. The M/IO- signal specifies whether a memory-mapped or I/O-mapped device or location is being addressed. Tables 1-5 and 1-6 list the system memory map and I/O map, respectively.

Table 1-5. System Memory Map

Address Range(h)	Allocated Space	Assigned Use (If Any)
000000-09FFFF	640 KB	System Board Memory (See Note 1)
0A0000-0BFFFF	128-KB Video Memory	Reserved Graphics Buffer Area
0C0000-0DFFFF	128-KB ROM	I/O Expansion ROM
0E0000-0EFFFF	64-KB ROM	System ROM Set 2 (Optional)
0F0000-0FFFFF	64-KB ROM	System ROM Set 1
100000-FDFFFF	15-MB RAM	Expansion Memory
FE0000-FFFFFF	128-KB ROM	Contents are the same as 0E0000-0FFFFF (See Note 2)

Notes: 1. The COMPAQ DESKPRO 286 with System Board Version 1 base memory is on the COMPAQ DESKPRO 286 System Memory Board. The memory for the PORTABLE 286 , the COMPAQ DESKPRO 286 with System Board Version 2, and the 12-MHz system board reside on the system memory board.

2. The system ROM can be addressed within either memory space. Memory decoding selects the ROM when these addresses are used. This arrangement is for software compatibility purposes.

Table 1-6. System I/O Map

	Range(h)	Function Addressed
SYSTEM BOARD	000-01F	DMA Controller 1
	020-03F	Interrupt Controller 1
	040-05F	Interval Timer (8254-2)
	060-06F	Keyboard Controller
	070-07F	Real-Time Clock, NMI
	080-08F	DMA Memory Page Register
	0A0-0BF	Interrupt Controller 2
	0C0-0DF	DMA Controller 2
	0F0	Clear 80287 Coprocessor
	0F1	Reset 80287 Coprocessor
	0F8-0FF	80287 Command Ports
CONTROLLER BOARDS	170-177	Fixed Disk Drive Controller 2
	1F0-1F7	Fixed Disk Drive Controller 1
	200-207	Game I/O
	278-27F	Parallel Port 3
	2F8-2FF	Serial Port 2 (COM2)
	300-31F	Not Used
	370-377	Multipurpose Drive or Multipurpose Fixed Disk Controller 2
	378-37F	Parallel Port 2
	380-38F	Not Used
	3A0-3AF	Not Used
	3B0-3DF	Video Display Controller
	3BC-3BF	LPT1
	3F0-3F7	Multipurpose Drive or Multipurpose Fixed Disk Controller 1
	3F8-3FF	Serial Port 1 (COM1)

Note: I/O address bits A<15..10> are not decoded.

1.8 SYSTEM FEATURES

The COMPAQ PORTABLE 286 and COMPAQ DESKPRO 286 have the following external features:

- Indicators
- Switches
- Security Lock
- Fuses
- Connectors

Indicators

Light-emitting diodes (LED) indicators show the activity or the state of the system. LED indicators are associated with the following devices:

- 1.2-Megabyte diskette drives have a two-color LED indicator. The light is red during read or write operations in the low-density mode (360-KB diskettes). The light is green during read or write operations in the high-density mode (1.2-Megabyte diskettes). The LED is white when no access is in progress.
- 360-Kbyte diskette drives and fixed disk drive backup systems have a LED indicator that lights when the drive is accessed.
- Fixed disk drives have a LED indicator that lights when the fixed disk drive is in use. The LED color depends on the fixed disk drive type.
- The keyboard has three LED indicators that show the current state of the CAPS LOCK, NUM LOCK, and SCROLL LOCK key functions.

Security Lock

Each system has a security lock on the front to prevent unauthorized use of the computer (also shown in figures 1-7 and 1-8). When the security lock is engaged, the computer ignores any input from the keyboard. The security lock on the COMPAQ DESKPRO 286 also serves as an interlock for the top cover.

Switches

Each system has a single AC power switch that turns all system power on or off. The COMPAQ PORTABLE 286 power switch is located on the left side of the system near the fan, as shown in Figure 1-9. The COMPAQ DESKPRO 286 power switch is located on the back right corner of the system, as shown in Figure 1-11.

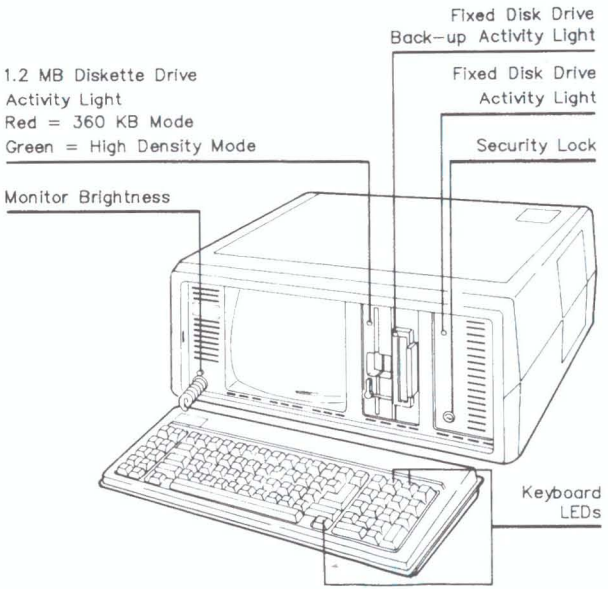

Figure 1-8. COMPAQ PORTABLE 286 Front View

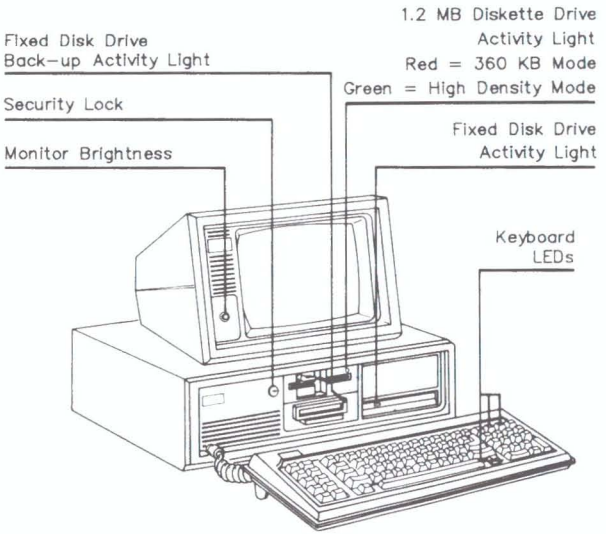

Figure 1-9. COMPAQ DESKPRO 286 Front View

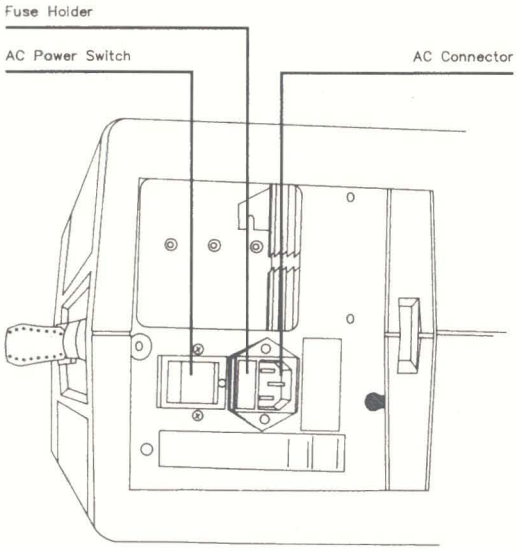

Figure 1-10. COMPAQ PORTABLE 286 Left Side View

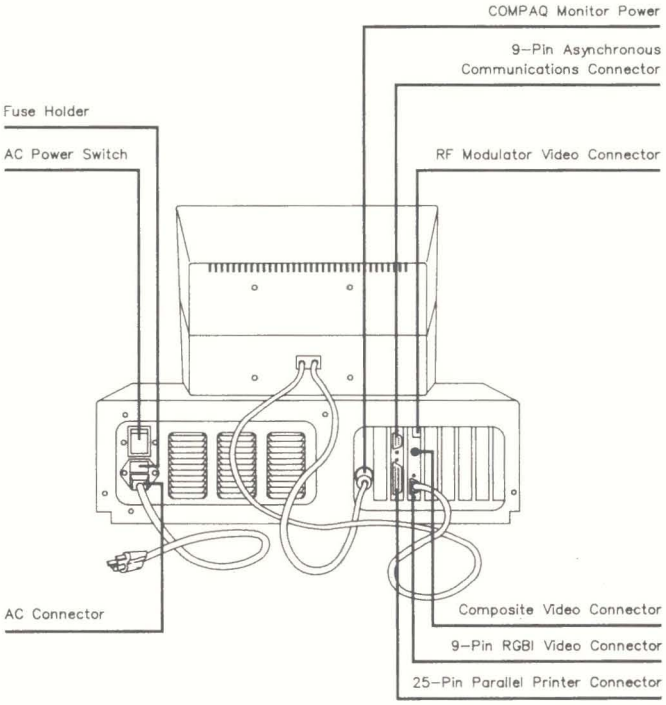

Figure 1-11. COMPAQ DESKPRO 286 Rear View

Fuses

Each system has a fuse on its AC power input for system protection. This fuse is in a removable housing that also contains a spare fuse, as shown in Figures 1-12 and 1-13.

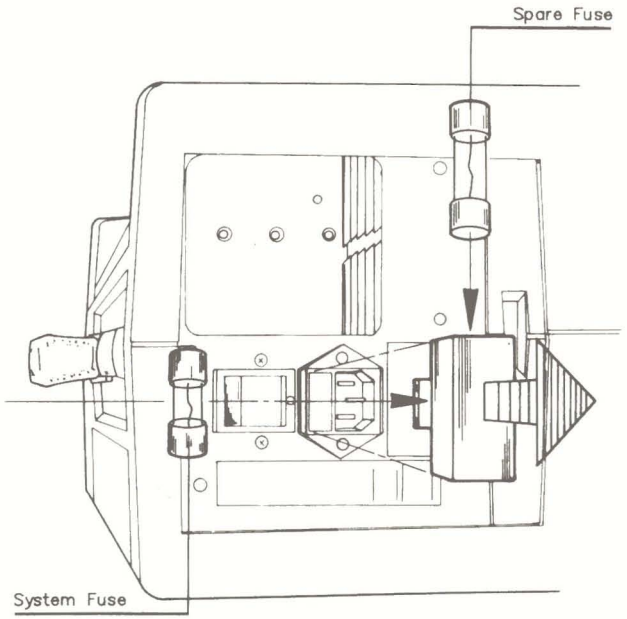

Figure 1-12. COMPAQ PORTABLE 286 Fuse Holder with Spare

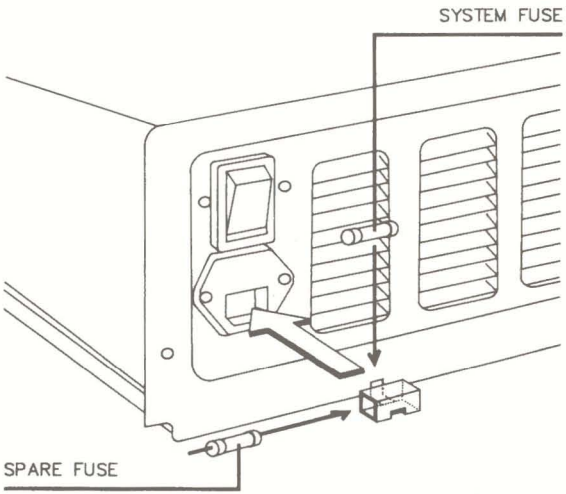

Figure 1-13. COMPAQ DESKPRO 286 Fuse Holder with Spare

Table 1-7 lists the fuse type required by each system.

Table 1-7. COMPAQ PORTABLE 286 and COMPAQ DESKPRO 286 Fuse Types

	COMPAQ PORTABLE 286	COMPAQ DESKPRO 286	COMPAQ DESKPRO 286 (12 MHz)
U.S.	3 A, 125 VAC	4 A, 125 VAC	5 A, 125 VAC
International	2.5 A, 250 VAC	2.5 A, 250 VAC	4 A, 250 VAC

1.9 CONNECTIONS

Each system has several connectors for peripheral devices, such as printers, modems, and monitors. Refer to Figure 1-11 for the locations of the COMPAQ DESKPRO 286 connectors. Refer to Figure 1-14 for the locations of the COMPAQ PORTABLE 286 connectors.

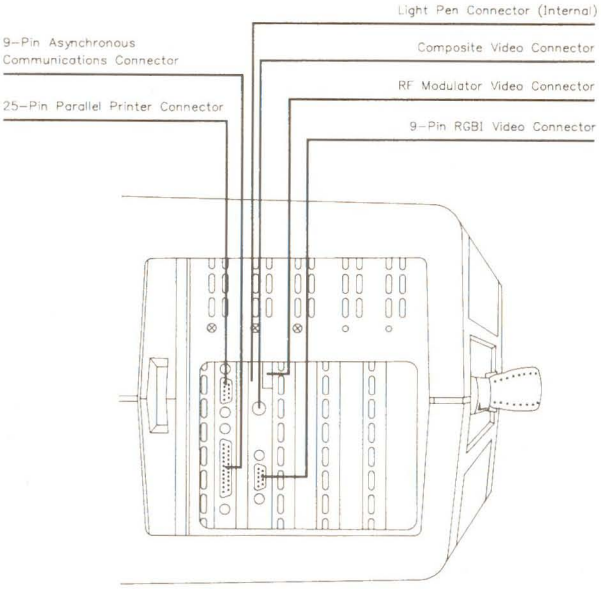

Figure 1-14. COMPAQ PORTABLE Right Side View

Chapter 2

SYSTEM BOARDS

Chapter 2
SYSTEM BOARDS

Chapter 2, Part 1

SYSTEM BOARDS (8 AND 6 MHz ONLY)

TABLE OF CONTENTS

CHAPTER 2
SYSTEM BOARDS

CHAPTER 2, PART 1
SYSTEM BOARDS (8 AND 6 MHZ ONLY)

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TABLE OF CONTENTS (Continued)

Chapter 2
SYSTEM BOARDS

2.1 INTRODUCTION

This chapter contains a block diagram discussion of the theory of operation for COMPAQ® personal computers with an 80286 Central Processing Unit (CPU) operating at 8- and 12-MHz. This chapter is divided into two parts to differentiate between the systems. The two parts are:

- PART 1: SYSTEM BOARDS (8- and 6- MHz Only)
- PART 2: SYSTEM BOARD (12-MHz Only)

Both parts of this chapter discuss CPU and CPU support circuitry, memory system, programmable devices, and expansion bus and bus functions as well as subsections discussing miscellaneous board information, jumpers, and connectors.

2.2 CPU AND CPU SUPPORT

The CPU and CPU support circuitry control and monitor the system.

The memory system controls access to and from the system Random Access Memory (RAM) and access from the system Read-Only Memory (ROM).

Programmable devices are hardware devices integrated on the system board that can be controlled or monitored by software.

The expansion bus and bus functions allow system access to hardware options that may be installed in the system. Hardware options may include display controllers, communications devices, and additional memory.

Also included in this chapter are discussions of:

- Miscellaneous System Board Information, such as fuses and indicators
- Jumpers
- Connectors
- Schematics

The 80286 microprocessor uses three busses, the 24-bit address bus, the 16-bit data bus, and the control bus to communicate with and control the system.

All devices outside the 80286 Central Processing Unit (CPU) are addressed either as memory-mapped devices or I/O-mapped devices.

The 80286 is reset when power is applied to the system board or after pressing the CTRL, ALT, and DEL keys simultaneously. After the CPU is reset, it addresses the ROM for instructions. The initial boot instructions in ROM check the system RAM and ROM for errors (checksums), and then initialize the system.

System initialization, or restart of the system, includes loading the programmable devices, such as the keyboard controller, the video controller, the RAM, and the with the desired starting values.

After initializing the system, the CPU loads the Disk Operating System (DOS) into memory from the diskette or fixed disk drive. The DOS is a program that manages and provides a consistent programming interface to the hardware.

Figure 2-1 is a functional block diagram of the 8- and 6-MHz system boards.

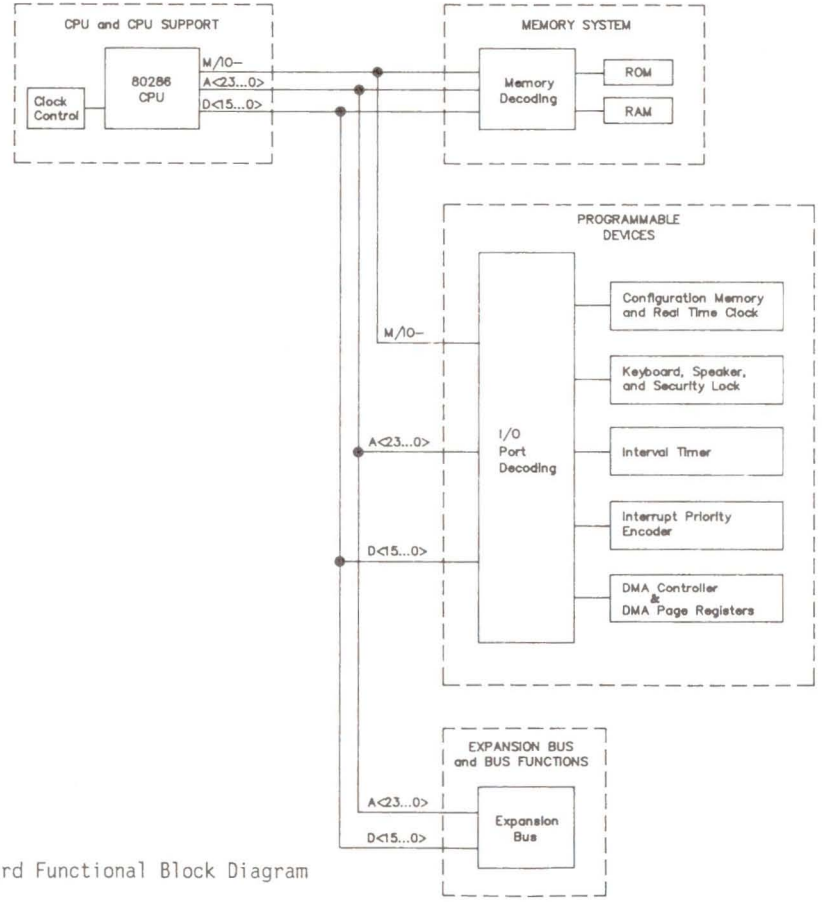


Figure 2-1. System Board Functional Block Diagram

Figure 2-2 shows a functional block diagram of the CPU and CPU support circuitry.

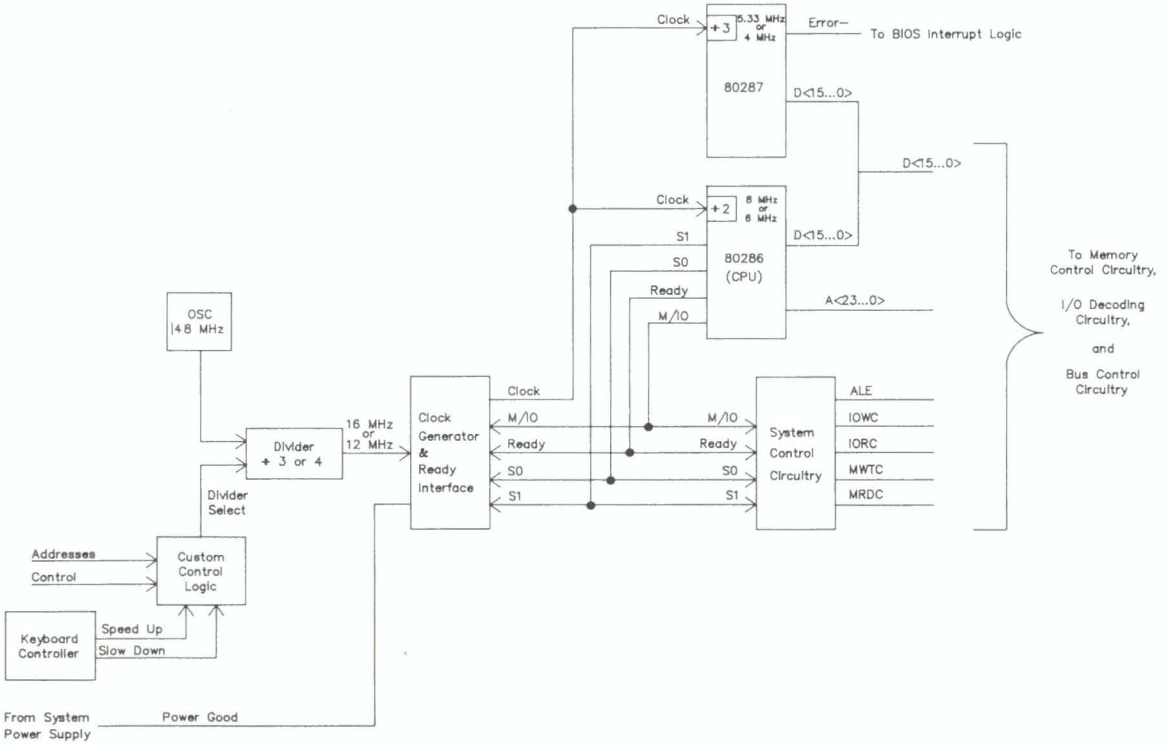


Figure 2-2. CPU and CPU Support Circuitry Block Diagram

Clock Generator and Ready Interface

The Clock Generator and READY Interface receives an input clock signal from an oscillator circuit and generates the clock signal for the 80286 CPU, the 80287 coprocessor, and the system control circuitry. The Clock Generator and READY Interface also monitors the power good (PWRGOOD) signal from the system power supply to control the system reset functions.

System Control Circuitry

The system control circuitry decodes the status signals S0, S1, and M/IO- (and other inputs such as CEN/AEN, READY-, et. al.) to control the system bus.

Table 2-1 shows the bus cycle status definition for the status signals.

Table 2-1. Bus Cycle Status Definition

M/IO-	S1	S2	Type of Bus Cycle
0	0	0	Interrupt Acknowledge
0	0	1	I/O Read (Ports)
0	1	0	I/O Write (Ports)
0	1	1	None: Idle
1	0	0	Halt or Shutdown
1	0	1	Memory Read
1	1	0	Memory Write
1	1	1	None: Idle

80287 Math Coprocessor (Optional)

The 80287 Math Coprocessor is a high-performance numeric processor extension of the 80286, adding floating point, extended integer, and BCD data-type support.

The 80287 automatically executes all numeric instructions as they are encountered. The 80287 responds to particular I/O addresses (00F8h, 00FAh, and 00FCh) that are automatically generated by the 80286.

The ERROR- signal of the 80287 is connected to IRQ13 (INT 75h). The BIOS interrupt handler for INT 75h routes this interrupt to INT 02h, which is the actual routine for coprocessor exceptions. This method is used to provide compatibility with 8088/8086 coprocessor exceptions and to prevent interference with the video I/O interrupt, INT 10h.

A socket is provided on the system boards for the 80287. A unique feature of the coprocessor is the ability to run at 4.0 or 5.33 MHz.

Clock Function

The COMPAQ 80286-Based Personal Computer products offer the choice of an 8MHz system clock for superior processing speed, or a 6MHz system clock to maintain compatibility with slower systems.

General Timing Information

The CPU status signals (S0, S1, and M/IO) are decoded by the CPU support circuitry to produce the command strobes used by the rest of the system (ALE, IOWC, IORC, MWTC, and MRDC).

2.3 MEMORY SYSTEM

Memory Address Decoding

The 80286 uses addresses <A23...A0> and control line M/IO- to specify memory locations. The address and control lines are decoded to specify memory areas for the system RAM and ROM.

Expansion boards such as memory, disk, or video must have their own devices to decode the I/O or memory space for that board.

Figure 2-3 shows a simplified block diagram of memory address decoding for the system board.

The memory decoder uses the REFRESH-, MRDC-, MWTC-, BALE, and LA23 to LA17 address lines to generate the MEM16-, RAM-, ROM-, RAS-, and CAS- signals.

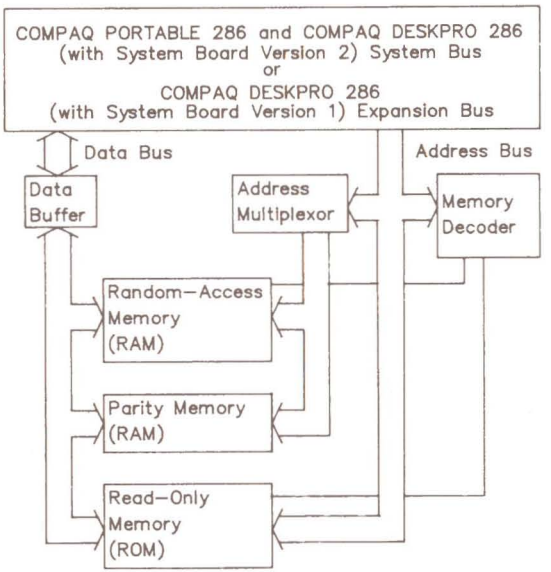


Figure 2-3. Memory Address Decoding Simplified Block Diagram

The 16-bit 80286 microprocessor (CPU) can read data from memory as bytes (8 bits), or words (16 bits). When a word on an an even boundary is read, an even numbered address is given by the CPU, and that address and the one above it are simultaneously read (Figure 2-4).

Two CPU cycles are required to read a word on an odd boundary. The next-lower even-numbered address is first given by the CPU, and the high-order byte of that location becomes the low-order 8 bits of the word. Then, the next-higher even-numbered address is given by the CPU, and the low-order byte of that location becomes the high-order 8 bits of the word.

Odd—numbered, High—order Byte	Even—numbered, Low—order Byte
Byte FFFFh (64K)	Byte FFFEh (64K—1)
.	.
.	.
.	.
Byte 0003h	Byte 0002h
Byte 0001h	Byte 0000h

Figure 2-4. A 16-Bit Word Divided into Two Bytes

Memory Support

Dynamic memory chips (RAM) require support circuitry to:

- Control the chips, using the CAS-, RAS-, and WR- signals
- Multiplex the address lines into the RAM
- Buffer the data lines
- Refresh the memory cells

The delay line generates the ENDRAS and STARTCAS signals and the signals that control the address multiplexing.

Two AM2966 chips buffer the address lines, and sequentially present the high- and low-order address lines to the RAM. The delay line controls the timing for this multiplexing operation.

Two 74LS245 chips buffer the data between the RAM and the data bus.

Memory refresh is accomplished by discrete circuitry. During memory refresh, every cell of every memory location is recharged.

COMPAQ PORTABLE 286 Memory System

The COMPAQ PORTABLE 286 system board has two banks for RAM (Bank 0 and Bank 1), two 16K x 8bit system ROMs, and two sockets for additional ROM. A bank of memory consists of 18 RAM devices located in two rows of 9.

COMPAQ PORTABLE 286 RAM

The COMPAQ PORTABLE 286 system board comes with 128 KB of RAM soldered in the first bank (Bank 0). The second bank (Bank 1) is socketed so that either 64K x 1-bit or 256K x 1-bit RAMs can be used.

Installing eighteen 64K x 1-bit RAMs in Bank 1 increases the total system board memory to 256 KB. Installing eighteen 256K x 1-bit RAMs in Bank 1 increases the memory to the maximum size of 640 KB.

If the COMPAQ PORTABLE 286 is purchased with 64K x 1-bit RAMs in Bank 1, then the jumper 'MS' is installed between pins 1 and 2 (Total RAM = 256KB). If 256K x 1-bit chips are used to replace the 64K x 1-bit chips in Bank 1, then move the jumper 'MS' to pins 2 and 3 (Total RAM = 640 KB).

If the COMPAQ PORTABLE 286 is purchased with 256K x 1bit RAMs in Bank 1, then the jumper 'MS' is installed between pins 2 and 3 (Total RAM = 640 KB).

In this model, a different decoding device (MEMPAL) is used, and when the jumper 'MS' is set between pins 1 and 2 the system disables the upper 128 KB of memory, reducing the total addressable RAM to 512 KB. This option is for use with certain software packages that will not run with more than 512 KB of system RAM.

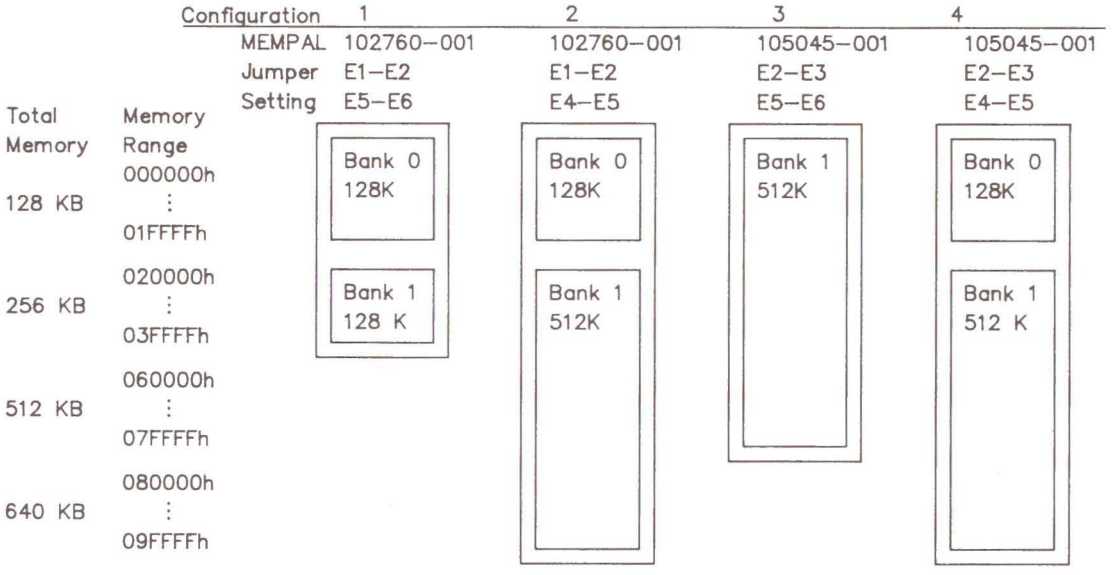
The system board uses approved 64K x 1-bit or 256K x 1-bit dynamic RAM devices with a response time of 150 ns or faster. (CAS access time must be 75 ns or faster.)

There are four possible memory configurations for the memory on the COMPAQ PORTABLE 286 system board:

1. 0-256 Kbytes using 64K x 1-bit dynamic RAMS (STANDARD Model 1).
2. 0-640 Kbytes by adding 256K x 1-bit dynamic RAMs to the Model 1.
3. 0-512 Kbytes using 256K x 1-bit dynamic RAMs, with Bank 0 disabled.
4. 0-640 Kbytes using 256K x 1-bit dynamic RAMs with all the memory enabled (STANDARD Model 2).

In every configuration, the lowest 128 KB of RAM is permanently installed (soldered in) as Bank 0.

Figure 2-5 shows the relationship between the memory map and the installed RAM.



Notes: 1. Configurations 2 and 4 are identical except for the MEMPAL type used.
2. For configuration 3, Bank 0 remains physically installed, but disabled. For this configuration only, address 000000h begins in Bank 1.

Figure 2-5. COMPAQ PORTABLE 286 Memory Configurations

COMPAQ PORTABLE 286 ROM

The COMPAQ PORTABLE 286 system board has four 28-pin sockets for ROM (or EPROM). The ROM sockets are addressed as two pairs, each 16 bits wide. The ROM pairs are designated ROM Set 1 (always present and including address OFFFF0h or FFFFF0h) and ROM Set 2 (located in the address space 64 KB below ROM Set 1).

ROM Set 1 contains the BIOS that initializes and controls the system. Installed in the ROM Set 1 sockets are 16K x 8-bit devices, one containing all even bytes and the other containing all odd bytes. The ROM Set 2 sockets are empty and provide for future enhancement.

ROMs can be, by pairs, either 8K, 16K, or 32K x 8-bit in size and may be either static and dynamic. Table 2-2 lists the jumper settings and resulting configuration for each type of ROM device.

Table 2-2. Jumper Settings for System ROMs

ROM Set 1 Jumper Settings			ROM Type
E13-E14	E10-E11	E16-E17	8Kx8, Static ROM, 250 ns
E14-E15	E10-E11	E16-E17	16Kx8, Static ROM, 250 ns
E13-E14	E11-E12	E16-E17	Invalid
E14-E15	E11-E12	E16-E17	32Kx8, Static ROM, 250 ns
E13-E14	E10-E11	E17-E18	8Kx8, Dynamic ROM, 150 ns
E14-E15	E10-E11	E17-E18	16Kx8, Dynamic ROM, 150 ns
E13-E14	E11-E12	E17-E18	Invalid
E14-E15	E11-E12	E17-E18	32Kx8, Dynamic ROM, 150 ns
ROM Set 2 Jumper Settings			**ROM Type**
E7-E8	E4-E5	E19-E20	8Kx8, Static ROM, 250 ns
E8-E9	E4-E5	E19-E20	16Kx8, Static ROM, 250 ns
E7-E8	E5-E6	E19-E20	Invalid
E8-E9	E5-E6	E19-E20	32Kx8, Static ROM, 250 ns
E7-E8	E4-E5	E20-E21	8Kx8, Dynamic ROM, 150 ns
E8-E9	E4-E5	E20-E21	16Kx8, Dynamic ROM, 150 ns
E7-E8	E5-E6	E20-E21	Invalid
E8-E9	E5-E6	E20-E21	32Kx8, Dynamic ROM, 150 ns

There are no jumper headers or plugs; the jumpers are etched on the solder side of the board in the following configurations:

ROM Set 1: 16K x 8-bit Static ROM (E14-E15, E10-E11, E16-E17)

ROM Set 2: 32K x 8-bit Dynamic ROM (E8-E9, E5-E6, E20-E21)

Changing the jumper settings requires cutting the conductors on the bottom side of the board to disconnect any unwanted jumpers, and soldering wire(s) to connect the jumpers as desired.

NOTE: Modifying these jumpers invalidates the COMPAQ warranty for this board.

SYSTEM ROM Set 1 occupies the 64 KB space at address 0F0000h through 0FFFFFh and identically at address FF0000h through FFFFFFh. SYSTEM ROM Set 2 occupies the 64 KB space at address 0E0000h through 0EFFFFh and identically at address FE0000h through FEFFFFh.

When 32K x 8-bit devices are used, the pair of ROMs fill the entire 64KB address space. When 16K x 8-bit devices are used, the most significant address bit is not decoded, so the ROMs are double mapped into two identical 32 KB sections of the 64 KB address space.

Similarly, when 8K x 8-bit devices are used, the two most significant address bits are not decoded, so the ROMs are mapped into four identical 16 KB sections of the 64 KB address space.

The system tests for the memory size as part of the Power-On Self-Test and compares this value with configuration memory. Errors detected cause the system to enter the SETUP program, if the diagnostic diskette or another diskette containing SETUP is installed.

COMPAQ DESKPRO 286 Memory System

The COMPAQ DESKPRO 286 Version 1 memory ROM and RAM are provided on a separate adapter board. See Chapter 3, "COMPAQ DESKPRO 286 System Memory Board" for more information.

The COMPAQ Deskpro 286 Version 2 system board has five banks for RAM, two 16K x 8-bit system ROMS, and two sockets for additional ROM.

COMPAQ DESKPRO 286 RAM

The COMPAQ DESKPRO 286 Version 2 System Board has 128 KB of RAM soldered in the first bank (Bank 0). The four remaining banks (Banks 1 through 4) are socketed so that either 64K x 1-bit or 256K x 1-bit RAMS may be used. Memory must be expanded in full-bank increments (18 RAM chips) in contiguous and ascending order, using the same RAM type (64K or 256K).

SW1 position 1 indicates the type of RAM in banks 1 through 4. When banks 1 through 4 are filled with 64K x 1-bit RAMS, SW1 position 1 must be CLOSED. When banks 1 through 4 are filled with 256K x 1-bit RAMS, SW1 position 1 must be OPEN.

NOTE: When SW1 position 1 is closed, positions 4 and 5 must both be open.

SW1 positions 2 and 3 limit the amount of base memory on the system board so that conflicts with expansion memory boards can be avoided. These two switches limit memory as shown in Table 2-3 regardless of the type of RAM in banks 1 through 4.

Table 2-3. Base Memory Size Switch Settings

SW1 Position 2	SW1 Position 3	(1) Total Base Memory	Address Range
CLOSED	CLOSED	Disabled RAM and ROM on System Board	
CLOSED	OPEN	256k	0-256 KB
OPEN	CLOSED	512k	0-512 KB
OPEN	OPEN	640k	0-640 KB

Notes: 1. Total Base Memory indicates maximum addressable base memory on the system board regardless of amount of RAM installed.
2. CLOSED = ON
OPEN = OFF

SW1 positions 4 and 5 enable/disable banks 2 through 4. These switches should be used to limit the amount of expansion memory on the system board when 256K x 1-bit RAMS are used to fill banks 1 through 4. (See Table 2-4).

Table 2-4. Expansion Memory Size Switch Settings

SW1 Pos 4	SW1 Pos 5	Banks Enabled	(1) Total Expansion Memory	Address Range
CLOSED	CLOSED	none	none	
CLOSED	OPEN	2	512K	1.0-1.5 MB
OPEN	CLOSED	2&3	1024K	1.0-2.0 MB
OPEN	OPEN	2,3,&4	1536K	1.0-2.5 MB

Notes: 1. Total Expansion Memory indicates maximum addressable expansion memory on the system board regardless of amount of RAM installed.
2. SW1 positions 4 and 5 should both be OPEN when 64K x 1-bit RAMS are used to fill banks 1 through 4 to ensure that SW1 positions 2 and 3 operate correctly.
3. CLOSED = ON
OPEN = OFF

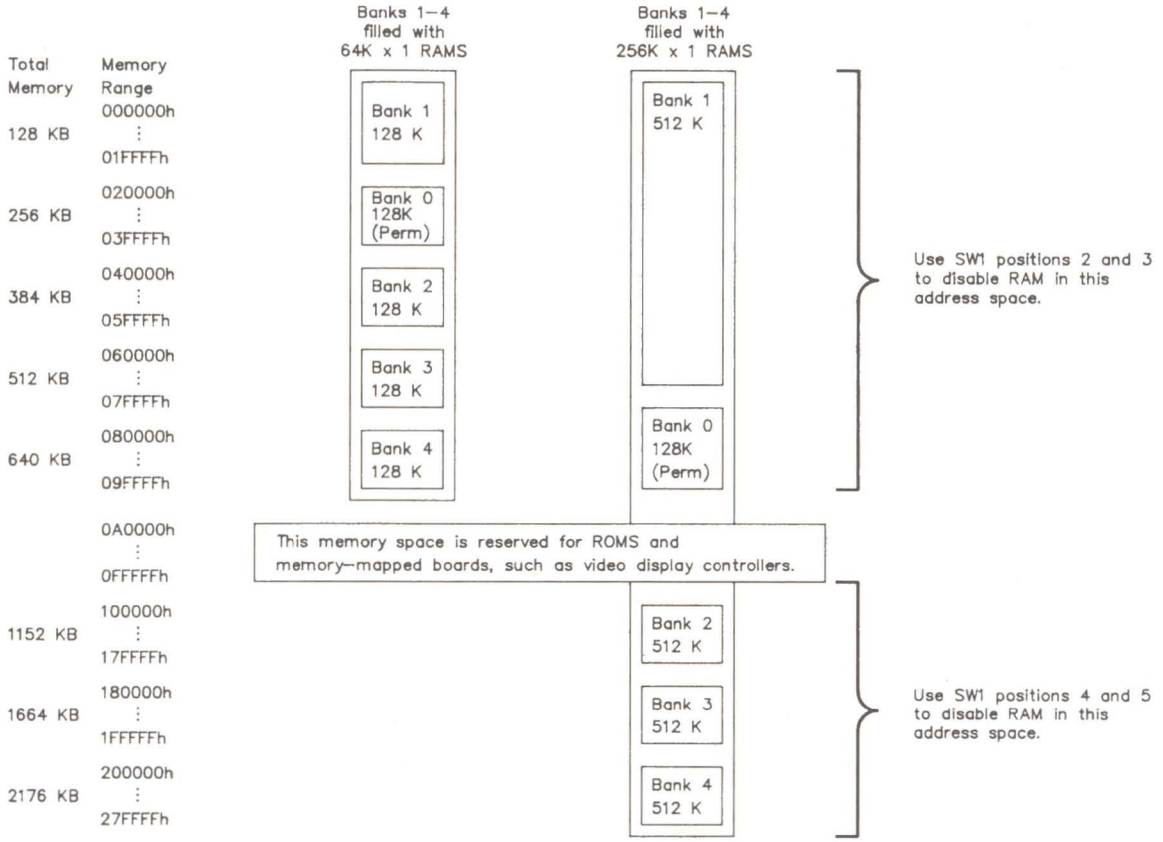


Figure 2-6. COMPAQ DESKPRO 286 Version 2 System Board Memory Configurations

The system board uses COMPAQ-approved 64K x 1-bit or 256K x 1-bit dynamic RAM devices with a response time of 150 ns or faster. (CAS access time must be 75 ns or faster.)

COMPAQ DESKPRO 286 Version 2 System Board ROM

The COMPAQ DESKPRO Version 2 System Board has four 28-pin sockets for ROM or EPROM. The ROM sockets are addressed as two pairs, each 16 bits wide and designated as ROM Set 1 (always present and including address 0FFFF0h or FFFFF0h) and system ROM SET 2 (located in the address space 64 KB below ROM Set 1).

ROM Set 1 controls the initial system operation (resetting and initializing the system). This code is known as the BIOS (Basic Input Output System). Installed in the two ROM Set 1 sockets are 16K x 8-Bit devices, one containing all even bytes and the other containing all odd bytes. The two ROM Set 2 sockets are empty and are provided for future expansion.

ROMs can be, by pairs, either 8K, 16K, or 32K x 8 bits in size and can be either static or dynamic. ROM Set 1 occupies the 64KB space at address 0F0000h through 0FFFFFh and identically at address FF0000h through FFFFFFh. ROM Set 2 occupies the 64 KB space at address 0E0000h through 0EFFFFh and identically at address FE0000h through FEFFFFh.

When 32K X 8-bit ROMs are used, the pair of ROMs fill the entire 64 KB address space. When 16K x 8-bit ROMs are used, the most-significant address bit is not decoded, so the ROMs are double-mapped into two identical 32 KB sections of the 64 KB address space.

Similarly, when 8K x 8-bit ROMs are used, the two most- significant address bits are not decoded, so the ROMs are quadruple-mapped into four identical 16 KB sections of the 64 KB address space.

Jumpers

Two jumpers (E1 and E2) are provided to enable use of a variety of types of ROM for special applications.

Table 2-5 shows the jumper settings and resulting configuration for each type of ROM.

Table 2-5. Jumper Settings for ROM Sets 1 and 2

ROM Set 1 = E1
ROM Set 2 = E2

Jumper Settings			ROM Type
1-2	4-5	7-8	8K x 8, Static ROM, 250 ns
2-3	4-5	7-8	16k x 8, Static ROM, 250 ns
1-2	5-6	7-8	Invalid
2-3	5-6	7-8	32k x 8, Static ROM, 250 ns
1-2	4-5	8-9	8k x 8, Dynamic ROM, 150 ns
2-3	4-5	8-9	16k x 8, Dynamic ROM, 150 ns
1-2	5-6	8-9	Invalid
2-3	5-6	8-9	32k x 8, Dynamic ROM, 150 ns

There are no jumper headers installed. The jumpers are etched on the solder side (bottom) of the board in the following configurations:

ROM Set 1:16K x 8-bit Static ROM (E1: 2-3, 4-5, 7-8)

ROM Set 2:32K x 8-bit Dynamic ROM (E2: 2-3, 5-6, 8-9)

Changing the jumper settings requires cutting the conductor on the solder side (bottom) of the board to disconnect any unwanted jumpers, then soldering wire(s) to jumpers as desired.

NOTE: Modifying these jumpers invalidates the COMPAQ warranty for this board.

2.4 PROGRAMMABLE DEVICES

The system BIOS controls the following system board programmable devices:

- Direct Memory Access (DMA) Controllers
- DMA Memory Page Register
- Real-Time Clock and Configuration Memory
- Keyboard Controller
- Interval Timer
- Interrupt Priority Encoder

These devices are all I/O mapped. Commands and opcodes are directed to the appropriate device by the I/O Port Decoding circuitry. Table 2-6 summarizes the port addresses used by the devices on the system board.

Table 2-6. System Board I/O Map

Port	Address Bits 9 8	7 6 5 4	3 2 1 0	Device
00h..0Fh	0 0	0 0 0 x	Y Y Y Y	8237A-5 Byte DMA Controller
20h..21h	0 0	0 0 1 x	x x x Y	8259A Interrupt Controller 1
40h	0 0	0 1 0 x	x x 0 0	8254-2 System Clock (Timer 0)
41h	0 0	0 1 0 x	x x 0 1	8254-2 Refresh Request (Timer 1)
42h	0 0	0 1 0 x	x x 1 0	8254-2 Speaker Tone (Timer 2)
43h	0 0	0 1 0 x	x x 1 1	8254-2 Command Mode Register
60h	0 0	0 1 1 0	x 0 x 0	8042 Date I/O Register
61h	0 0	0 1 1 0	x x x 1	Port B/C Input/Outputs
64h	0 0	0 1 1 0	x 1 x 0	8042 Status/Command Register
70h	0 0	0 1 1 1	x x x 0	RTC Address Register (bits <5..0>)
70h	0 0	0 1 1 1	x x x 0	NMI Enable Register (bit <7>)
71h	0 0	0 1 1 1	x x x 1	RTC Data I/O Register
80h	0 0	1 0 0 x	0 0 0 0	DMA Page Register Spare
81h	0 0	1 0 0 x	0 0 0 1	DMA Page Register CH 2 Page
82h	0 0	1 0 0 x	0 0 1 0	DMA Page Register CH 3 Page
83h	0 0	1 0 0 x	0 0 1 1	DMA Page Register CH 1 Page
84h	0 0	1 0 0 x	0 1 0 0	DMA Page Register Spare
85h	0 0	1 0 0 x	0 1 0 1	DMA Page Register Spare
86h	0 0	1 0 0 x	0 1 1 0	DMA Page Register Spare
87h	0 0	1 0 0 x	0 1 1 1	DMA Page Register CH 0 Page
88h	0 0	1 0 0 x	1 0 0 0	DMA Page Register Spare

(Continued)

Table 2-6. (Continued)

Port	Address Bits 9 8	7 6 5 4	3 2 1 0	Device
89h	0 0	1 0 0 x	1 0 0 1	DMA Page Register CH 6 Page
8Ah	0 0	1 0 0 x	1 0 1 0	DMA Page Register CH 7 Page
8Bh	0 0	1 0 0 x	1 0 1 1	DMA Page Register CH 5 Page
8Ch	0 0	1 0 0 x	1 1 0 0	DMA Page Register Spare
8Dh	0 0	1 0 0 x	1 1 0 1	DMA Page Register Spare
8Eh	0 0	1 0 0 x	1 1 1 0	DMA Page Register Spare
8Fh	0 0	1 0 0 x	1 1 1 1	DMA Page Register Refresh Page
A0h..A1h	0 0	1 0 1 x	x x x Y	8259A Interrupt Controller 2
C0h..CFh	0 0	1 1 0 Y	Y Y Y x	8237A-5 Word DMA Controller
F0h	0 0	1 1 1 x	0 x x 0	Clear Math Processor Busy
F1h	0 0	1 1 1 x	0 x x 1	Reset Math Processor
F8h..FFh	0 0	1 1 1 1	1 Y Y x	80287 Command Ports

Notes: 1. x = Don't care. The value of these bits does not affect the I/O address decoding.
2. Y = Register dependent.

I/O Port Decoding

The 80286 uses address (A<15...0>) and control lines (M/IO-) to specify I/O operations. Although the 80286 uses 16 bits for an I/O address, the system board and expansion boards use only 10 bits (A<9...0>), therefore I/O space is limited to 3FFh. The address and control lines are decoded to specify I/O and addresses for the system board I/O-mapped devices (DMA controllers, real-time clock, interval timer, etc.).

Expansion boards such as memory, disk, and video must have their own devices to decode the I/O-mapped devices for that board. Figure 2-7 shows a simplified block diagram of I/O port decoding for the system board.

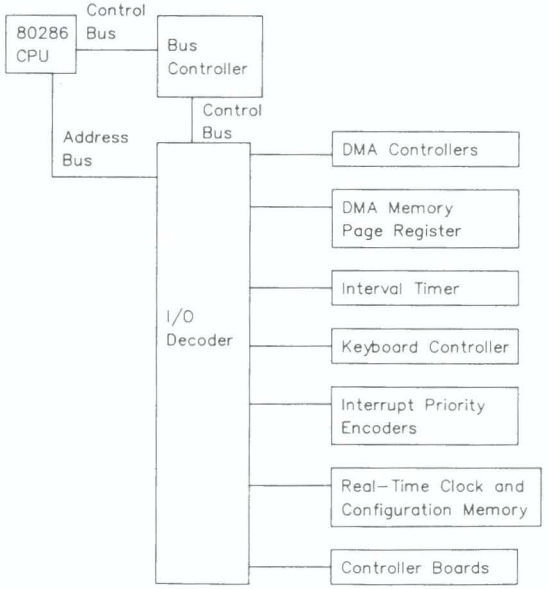


Figure 2-7. I/O Address Decoding Simplified Block Diagram

Direct Memory Access Controller

Direct Memory Access (DMA) is a method of directly accessing memory without involving the CPU. DMA is normally used to transfer blocks of data to or from an I/O device. DMA reduces the amount of CPU interactions with memory, freeing the CPU for other processing tasks.

The system board uses two Intel 8237 DMA controllers, with four bidirectional data channels each. The DMA controllers operate at half the system clock rate (8 MHz/2 or 4 MHz/2). Table 2-7 lists the function assigned to each DMA channel.

Table 2-7. DMA Channels Assigned to the Controllers

Controller 1 (Byte Transfers)	
Channel	Function
0	Spare
1	SDLC (Communications)
2	Diskette Data Transfers
3	Spare
Controller 2 (Word Transfers)	
Channel	Function
4	Cascade for Controller 1
5	Spare
6	Spare
7	Spare

The DMA controllers hold (or define) only 16 bits of the 24-bit address. The other 8 address bits are contained in the DMA Memory Page Register (74LS612) or MAP Gate Array. See the "DMA Memory Page Register" section for more information.

DMA Controller 1 is used for byte (8-bit) data transfers (Figure 2-8). DMA Controller 2 is used for word (16-bit) data transfers. Unlike the CPU, DMA Controller 2 can only transfer words on an even boundary.

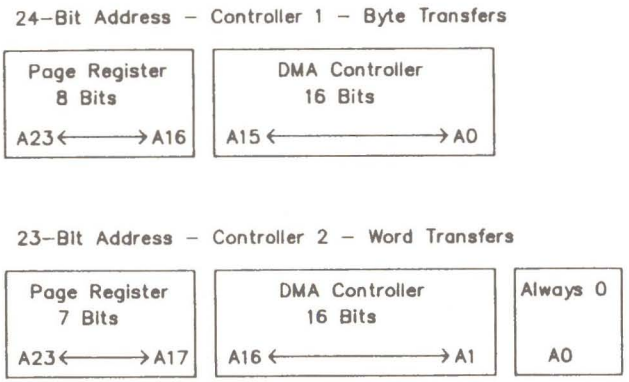


Figure 2-8. Memory Address Derived from Page Register and DMA Register Contents

A16 from the DMA memory page register is disabled when DMA Controller 2 is selected. A0 is not connected to DMA Controller 2. A0 is always 0 when word-length transfers are selected. This arrangement (not connecting A0) means that the size of the block of data that can be moved or addressed is measured in 16-bit words, rather than 8-bit bytes.

Since the DMA controllers only contain 16 bits of the 24-bit address, they can only move blocks of data within their ability to address that data.
DMA Controller 1 can move up to 64K bytes of data.
DMA Controller 2 can move up to 64K words, or 128K bytes of data.

The DMA controllers are complex devices with several registers for commands and status. Table 2-8 shows the I/O-map and the commands and formats of the registers.

Transferring Data from I/O Devices to Memory

DMA controllers and I/O devices use the DRQx and DAKx signals as "handshaking". When an I/O device has a byte or word of data to send, the I/O device makes its DRQx line active. When the DAKx line from the DMA controller goes active, the device puts its data on the data bus.

Transferring Data from Memory to Memory

The hardware does not support memory-to-memory block transfers.

NOTE: After power-on, it is recommended that all command, mode, and mask registers be loaded with valid values to ensure proper operation of the device.

Table 2-8. DMA Controller Registers

Register Function	Bits	Port Addresses Cntlr 1	Cntlr 2	Read/Write
Status	8	08h	D0h	Read
Command	8	08h	D0h	Write
Mode	6	0Bh	D6h	Write
Write Single Mask Bit	4	0Ah	D4h	Write
Write All Mask Bits	4	0Fh	DEh	Write
Software DRQx Request	4	09h	D2h	Write
Base And Current Address - CH 0	16	00h	C0h	Write
Current Address - CH 0	16	00h	C0h	Read
Base & Current Word Count - CH 0	16	01h	C2h	Write
Current Word Count - CH 0	16	01h	C2h	Read
Base And Current Address - CH 1	16	02h	C4h	Write
Current Address - CH 1	16	02h	C4h	Read
Base & Current Word Count - CH 1	16	03h	C6h	Write
Current Word Count - CH 1	16	03h	C6h	Read
Base And Current Address - CH 2	16	04h	C8h	Write
Current Address - CH 2	16	04h	C8h	Read
Base & Current Word Count - CH 2	16	05h	CAh	Write
Current Word Count - CH 2	16	05h	CAh	Read
Base And Current Address - CH 3	16	06h	CCh	Write
Current Address - CH 3	16	06h	CCh	Read
Base & Current Word Count - CH 3	16	07h	CEh	Write

Note: See "RESET POINTER FLIP-FLOP" for an explanation of 16-bit data transfers to the DMA controllers.

(Continued)

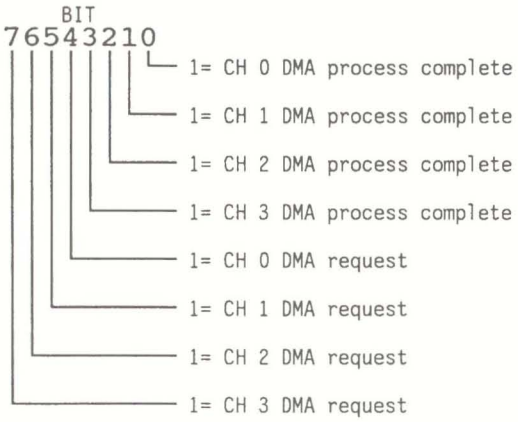
Table 2-8. (Continued)

Register Function	Bits	Port Addresses Cntrl 1	Cntrl 2	Read/Write
Current Word Count - CH 3	16	07h	CEh	Read
Temporary	16	0Dh	DAh	Read
Reset Pointer Flip-flop	(Note 1)	0Ch	D8h	Write
Master Reset	(Note 1)	0Dh	DAh	Write
Reset Mask Register	(Note 1)	0Eh	DCh	Write

Notes: 1. This is not a register, but a direct command to the DMA Controller.
2. See "RESET POINTER FLIP-FLOP" for an explanation of 16-bit data transfers to the DMA controllers.

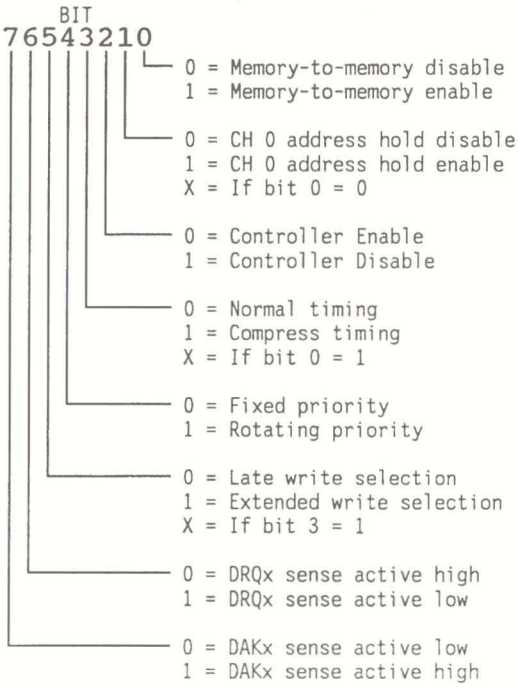
STATUS

The Status register bits are set (= 1) to indicate that a channel has requested DMA access or that a DMA process is complete.



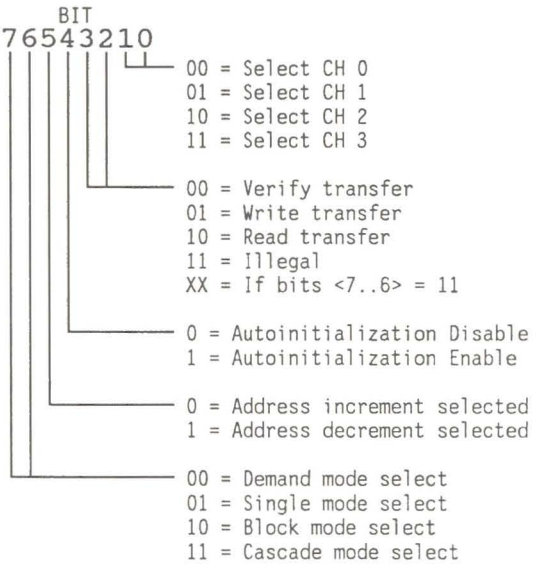
COMMAND

The command register bits control the DMA operation. All bits are reset (=0) by the master clear instruction or a system reset. This register must be programmed to 00 for proper system operation.



MODE

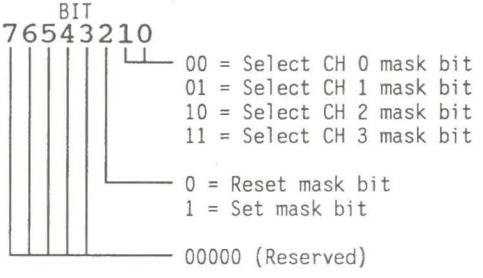
Each channel has a 6-bit register associated with it. The first two bits of the byte written to this register specify which channel is being selected. These registers specify the operating mode for each channel.



If the BLOCK or DEMAND mode is selected for a channel, the total transfer time must not exceed 15 us or RAM will not be properly refreshed.

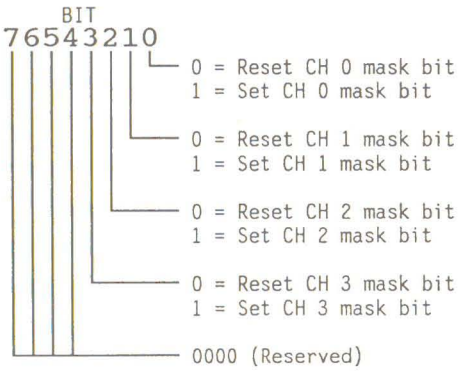
WRITE SINGLE MASK BIT

This command sets (=1) or resets (=0) a single mask bit. When a mask bit is set, that channel's DRQx is disabled. The "WRITE ALL MASK BITS" command can set or reset all the mask bits.



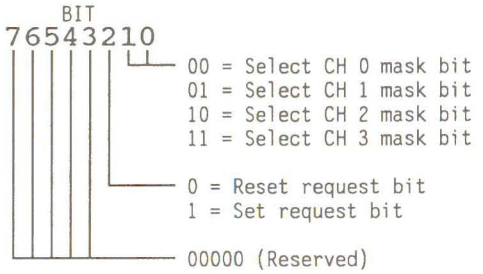
WRITE ALL MASK BITS

This command sets (=1) or resets (=0) all the mask bits. When a bit is set, that channel's DRQx is disabled. The "WRITE SINGLE MASK BIT" command can set or reset a single mask bit.



SOFTWARE DRQx REQUEST

The DMA controller can respond to software requests for DMA as well as hardware requests from DRQx lines. The channel must be in the block mode, and the appropriate registers (base addresses and so forth) must be set before initiating this request.



BASE AND CURRENT ADDRESS - CHANNELS 0-3

These 16-bit registers specify the starting destination address for the memory transfer. This is a write-only register. The 16-bit contents are loaded into these registers as a two-part operation. The first write to this register loads the eight least-significant bits. The second consecutive write loads the eight most-significant bits. See the "RESET POINTER FLIP-FLOP" command.

CURRENT ADDRESS CHANNELS 0-3

These 16-bit registers specify either the current address, or the destination address for the next data transfer. This address is the same as the base address, plus address increments or decrements made after each data transfer. These are read-only registers. The 16-bit contents are read from these registers as a two-part operation. The first read from this register returns the eight least-significant bits. The second consecutive read returns the eight most-significant bits. See the "RESET POINTER FLIP-FLOP" command.

BASE AND CURRENT WORD COUNT - CHANNELS 0-3

These 16-bit registers specify the number of words to be transferred. This is a write-only register. The 16-bit contents are loaded into these registers as a two-part operation.

The first write to this register loads the eight least-significant bits. The second consecutive write loads the eight most-significant bits. See the "RESET POINTER FLIP-FLOP" command.

CURRENT WORD COUNT - CHANNELS 0-3

These 16-bit registers specify the number of words already moved as part of a data block. These are read-only registers. The 16-bit contents are read from these registers as a two-part operation. The first read from this register returns the eight least- significant bits. The second consecutive read returns the eight most-significant bits. See the "RESET POINTER FLIP-FLOP" command.

TEMPORARY

This register is not used in this hardware configuration.

RESET POINTER FLIP-FLOP

This is a direct command to the DMA controller to reset the pointer flip-flop that keeps track of 16-bit data transfers. This command is given to reset the pointer to a known state so that the DMA controller will load the high- and low-order bytes in the proper sequence. Use this command before writing a 16-bit base address or other 16-bit command or data to the DMA controller.

MASTER RESET

This is a direct command to the DMA controller to reset the DMA controller It has the same effect as a hardware reset; the command, status, request, temporary, and pointer flip-flop registers are reset (=0), and the mask register bits are set (=1).

RESET MASK REGISTER

This is a direct command to the DMA controller to reset the mask register, enabling all four channels to receive DRQs (data requests).

DMA Memory Page Register

The DMA memory page register contains the eight most significant bits of the 24-bit address. It works in conjunction with the DMA controllers to define the complete (24-bit) address for the DMA channels. Table 2-9 shows the port address assigned to each page register. See the section on the DMA controllers for more information.

Table 2-9. Port Address For DMA Channels

DMA Channel	Page Register I/O Port Address
0	087h
1	083h
2	081h
3	082h
4	None
5	08Bh
6	089h
7	08Ah
Refresh	08Fh (See Note)

Note: The DMA memory page register for the refresh channel must be programmed with 00h for proper system operation.

Real-Time Clock and Configuration Memory

The COMPAQ 286 family computer system boards use the Motorola MC146818 device as their Real-Time Clock (RTC) and Configuration Memory. This device has a total of 64 bytes of memory. The first fourteen memory locations are used for the RTC. The remaining 50 memory locations are used for the system configuration.

A value can be written to or read from all 64 registers except:

- Status Registers C and D, which are read-only
- Bit 7 of Status Register A, which is read-only
- The high-order bit of the seconds byte, which is read-only

Figure 2-9 shows the memory map for the MC146818.

To prevent a loss of time or system configuration, the MC146818 uses power obtained from a battery mounted on the inside of the computer. The battery maintains the time and system configuration during power loss for up to three years. The system does NOT charge the battery.

NOTE: If the battery is disconnected or fails for any reason, the time and system configuration must be reprogrammed into the MC146818.

To reset the time or system configuration, run the SETUP procedure found on the USER'S PROGRAM diskette or on the Advanced Diagnostics Diskette. To reset the time, use either the SETCLOCK (DOS) command, or the appropriate INT 1Ah (BIOS) command.

The MC146818 is an I/O mapped device. Use the 80286 OUT and IN instructions to read or write to the memory in this device. Note that the port 70h is shared between the NMI mask register and the configuration memory address register. To leave the NMI mask enabled, make sure that bit 7 is set to 0 when writing a RTC address to port 70h.

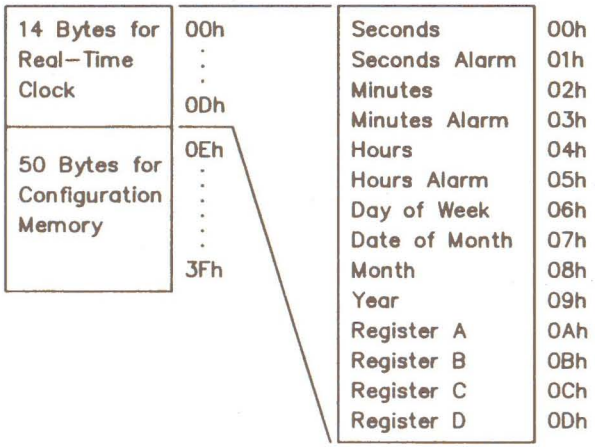


Figure 2-9. MC146818 Memory Map

To write a value into memory:

1. Use OUT 70h, AL to specify the memory location to change. 70h is the port number; AL is the memory location.
2. Use OUT 71h, AL to specify the data for the memory location. 71h is the port number; AL is the data.

To read the contents of a memory location:

1. Use OUT 70h, AL to specify the memory location to read. 70h is the port number; AL is the memory location.
2. Use IN AL, 71h to read data stored in that location. The returned data is placed in the AL register of the 80286.

Table 2-10 summarizes the types of information stored in the MC146818's memory locations.

Table 2-10. MC146818 Real-Time Clock Memory Locations

Register	Function
00h	Seconds
01h	Seconds Alarm
02h	Minutes
03h	Minutes Alarm
04h	Hour
05h	Hour Alarm
06h	Day of Week
07h	Day of Month
08h	Month
09h	Year
0Ah	Status Register A
0Bh	Status Register B
0Ch	Status Register C
0Dh	Status Register D
0Eh	Diagnostic Register
0Fh	Reset Code Byte
10h	Diskette Drive Type
11h	Reserved
12h	Fixed Disk Drive Type
13h	Reserved
14h	Equipment Installed
15h,16h	System Board Memory Size
17h,18h	Extended Memory Installed

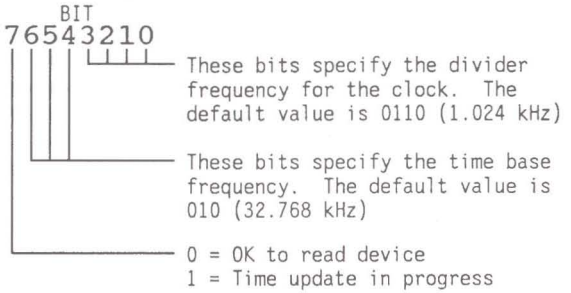
(Continued)

Table 2-10. (Continued)

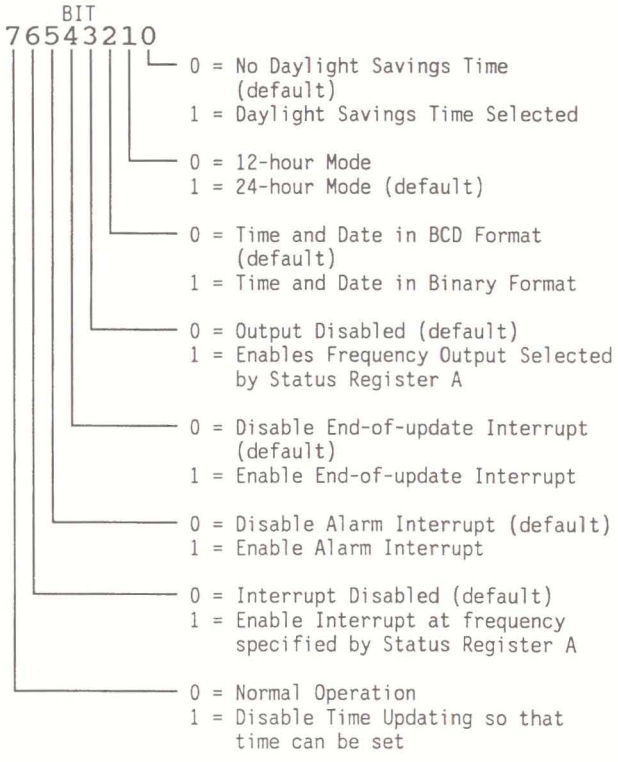
Register	Function
19h-2Ch	Reserved
2Dh	Additional Flags
2Eh,2Fh	Checksum Value
30h,31h	Memory More than 1 MB
32h	Century, part of time and date function
33h	System Information
34h-3Fh	Reserved

Information about registers 0Ah through 33h follows.

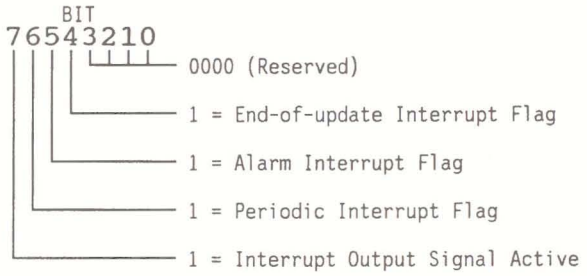
STATUS REGISTER BYTE 0Ah



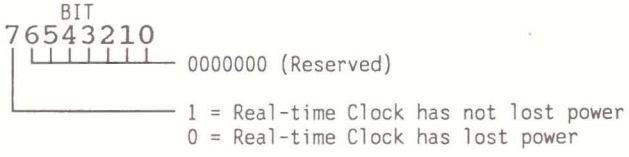
STATUS REGISTER BYTE 0Bh



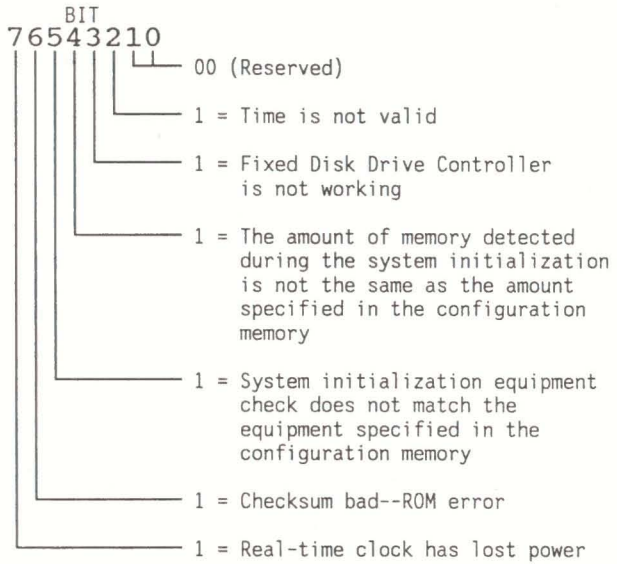
STATUS REGISTER BYTE 0Ch--READ-ONLY



STATUS REGISTER BYTE 0Dh

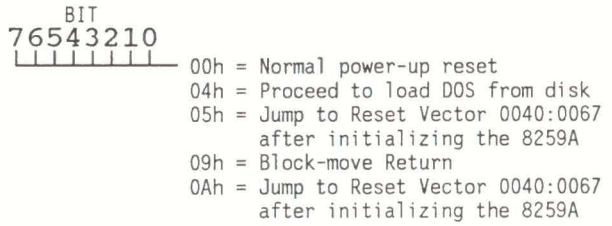


CONFIGURATION BYTE 0Eh--DIAGNOSTIC STATUS BYTE



CONFIGURATION BYTE 0Fh--RESET CODE BYTE

The reset code tells the system what to do after the CPU is reset. The reset code identifies the type of, or reason for, reset. The reset code also provides a method of resetting the system without losing previously-stored data or to return the system to the Real Mode from the Protected Virtual Memory Mode.

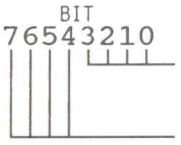


CONFIGURATION BYTE 10h--DISKETTE DRIVE TYPE

Secondary Diskette Drive Type
(use values given below)

Primary Diskette Drive Type:
0000 = No diskette drive
0001 = 360-Kbyte Diskette Drive
0010 = 1.2-Megabyte Diskette Drive
0011 = Reserved
:
1111 = Reserved

CONFIGURATION BYTE 12h--FIXED DISK DRIVE TYPE



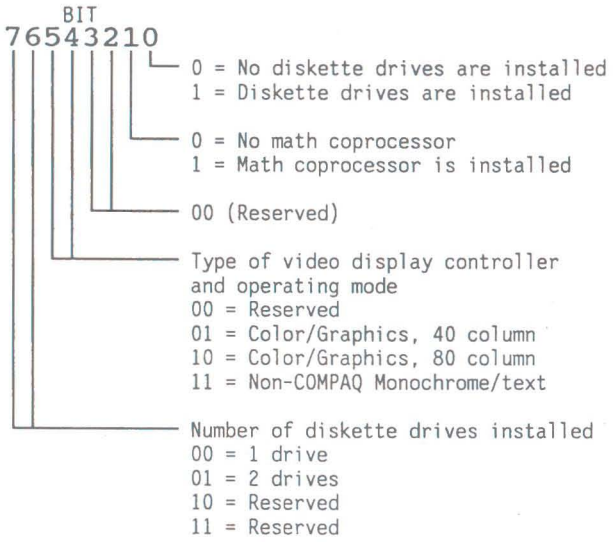
Value defines second fixed disk dirve type
(use table below)

Values defines fixed disk drive type:

Value	Size	System
0000	None	
0010	20-MB	COMPAQ PORTABLE 286
0010	20-MB	COMPAQ DESKPRO 286
0110	30-MB	COMPAQ DESKPRO 286
1100	70-MB	COMPAQ DESKPRO 286

NOTE: This byte identifies the type of fixed disk drive used, not the capacity.

CONFIGURATION BYTE 14h--EQUIPMENT INSTALLED



CONFIGURATION BYTES 15h AND 16h--BASE MEMORY SIZE

Value indicates valid memory sizes for the base memory size:

Byte 16h	Byte 15h	Memory Size
00h	80h	128 KB
01h	00h	256 KB
02h	00h	512 KB
02h	80h	640 KB

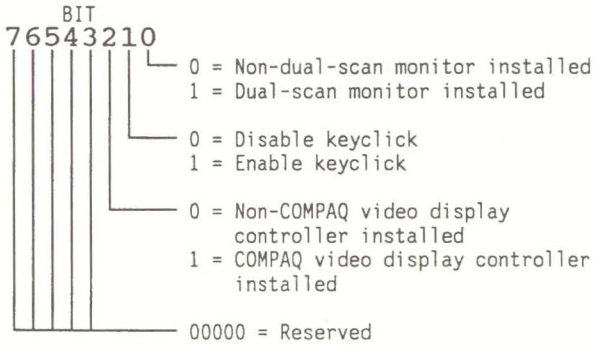
CONFIGURATION BYTES 17h AND 18h--MEMORY AMOUNT

Value indicates valid memory sizes for memory on all memory option boards:

Byte 18h	Byte 17h	Memory Size
02h	00h	512 KB
04h	00h	1024 KB
06h	00h	1536 KB
.	.	
.	.	
3Bh	80h	15232 KB

CONFIGURATION BYTE 2Dh--ADDITIONAL FLAGS

This byte allows the configuration of special features.



CONFIGURATION BYTES 2Eh AND 2Fh--MEMORY CHECKSUM

Value stored is the checksum for memory addresses 10h..2Dh.

Byte 2Eh = High byte of checksum

Byte 2Fh = Low byte of checksum

CONFIGURATION BYTES 30h AND 31h--MEMORY OVER 1 MB

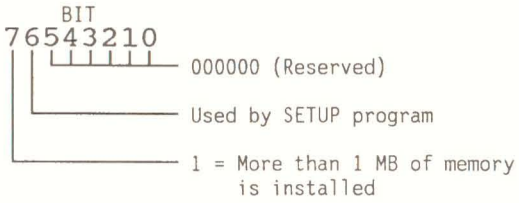
Value indicates amount of system memory in excess of 1 MB. These bytes are updated by the BIOS at power-on.

Byte 31h	Byte 30h	Memory Size
02h	00h	512 KB
04h	00h	1024 KB
06h	00h	1536 KB
08h	00h	2048 KB
0Ah	00h	2560 KB
0Ch	00h	3072 KB
0Eh	00h	3584 KB
10h	00h	4096 KB
12h	00h	4608 KB
14h	00h	5120 KB
16h	00h	5632 KB
18h	00h	6144 KB
1Ah	00h	6656 KB
1Ch	00h	7168 KB
1Eh	00h	7680 KB
.	.	.
.	.	.
3Bh	80h	15232 KB

CONFIGURATION BYTE 32h--DATE, CENTURY

This is the century part of the current time and date encoded in BCD (binary coded decimal). The BIOS sets and reads this value.

CONFIGURATION BYTE 33h--SYSTEM INFORMATION



Keyboard Controller

An INTEL 8042 single-chip microcomputer provides:

- An output port for system function control and keyboard communication
- An input port to read system function status
- A test port to read the status of the keyboard clock and data lines

The 8042 has internal ROM that is custom-programmed with keyboard scan codes and operating instructions. Figure 2-10 shows a simplified block diagram of the keyboard controller.

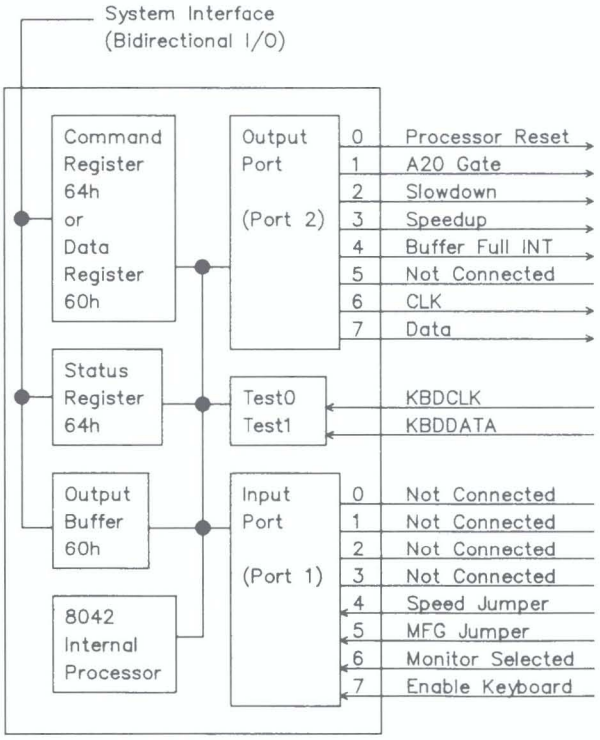


Figure 2-10. Keyboard Controller Functional Block Diagram

The 8042 communicates with the keyboard in a bidirectional, serial format with a synchronizing clock. The 8042 receives serial data, checks its parity, translates the 11- or 9-bit scan codes from the keyboard into system codes, and interrupts the 80286 to transfer data into the system.

Command codes between the 8042 and the keyboard are described in Chapter 8.

The 8042-to-Keyboard Interface

The 8042 and the keyboard are connected by a four conductor, shielded cable that carries a power line, a ground line, a data signal, and a clock signal.

The 8042 and the keyboard communicate in a handshaking fashion, using the data and clock lines for synchronous serial communication. The data and clock lines are driven by open-collector drivers at both ends of the cable in a wired-OR fashion.

The keyboard supplies the synchronizing clock for data transmissions in either direction.

Figure 2-11 shows a simplified schematic of the data and clock circuits.

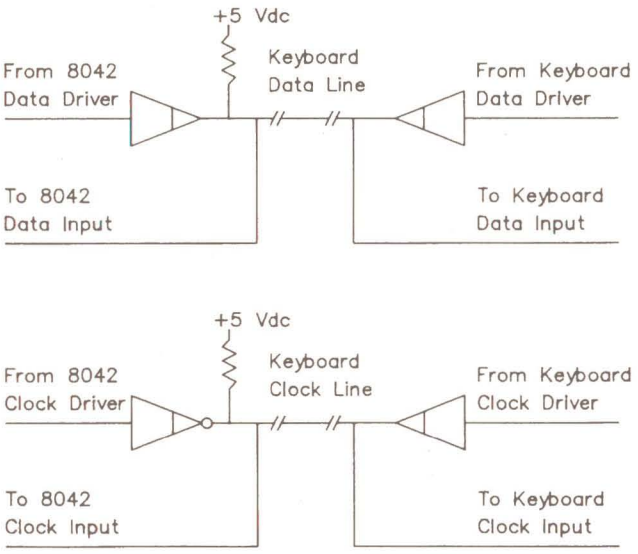
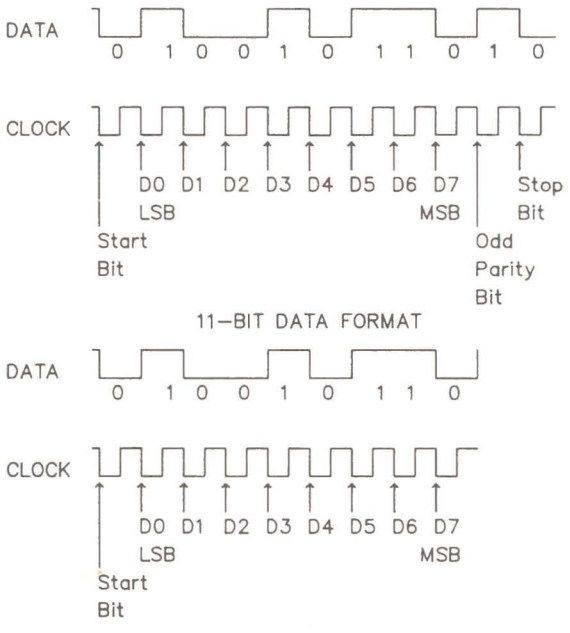


Figure 2-11. Simplified Schematic of the Data and Clock Circuits

11- or 9-Bit Data Transmission Format

The 8042 adds versatility to the system by allowing 11- or 9- bit keyboards to be used interchangeably at any time. The system sends commands to the 8042 to specify the type of scan code it expects, and the 8042 sends that type of scan code, regardless of the type of keyboard connected.

The 8042 automatically tests for keyboard type by monitoring the data format. Figure 2-12 shows 11- and 9- bit data formats with sample data transfers.



Note: The keyboard drives the data line low for the Stop Bit at the end of a transmission to acknowledge the transmission.

Figure 2-12. 11- and 9-Bit Data Formats

Table 2-11 lists the 11- and 9-bit data transfer timing parameters.

Table 2-11. Keyboard Data Timing Parameters

Parameter	11-Bit	9-Bit
Clock timing (min.), Falling edge to falling edge	60 us	25 us
Clock timing (min.), Falling edge to rising edge	5 us	5 us
Transmission Time (max.) First edge to completion	2 us	2 us
Time data must be valid before falling clock edge	0 us	0 us
Time data must be valid after falling clock edge	5 us	12 us

8042 Port Functions

The 8042 has three ports:

- An 8-bit output port for system function control and keyboard communication
- An 8-bit input port to read system function status
- A 2-bit test port to read the status of the keyboard clock and data lines.

To write to the output port:

1. Write command D1h (next byte is a value byte) to I/O address 64h.
2. Write the desired value for the output port to port address 60h.

To read the 8042 output port value:

1. Write command D0h (transfer the current output port values to the 8042 output buffer) to port address 64h.
2. Read the 8042 output buffer (port address 60h).

Figure 2-13 shows the bit values for the output port of the 8042.

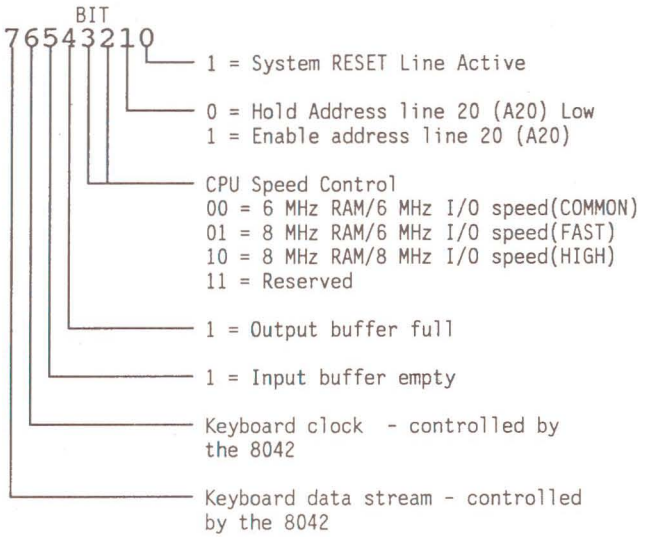


Figure 2-13. 8042 Output Port - Bit Definition

To read the 8042 input port value:

1. Write command C0h (transfer the current input port values to the 8042 output buffer) to I/O address 64h.
2. Read the 8042 output buffer (port address 60h) with the special read command A5h.

Figure 2-14 shows the format of the byte returned from the 8042 input port.

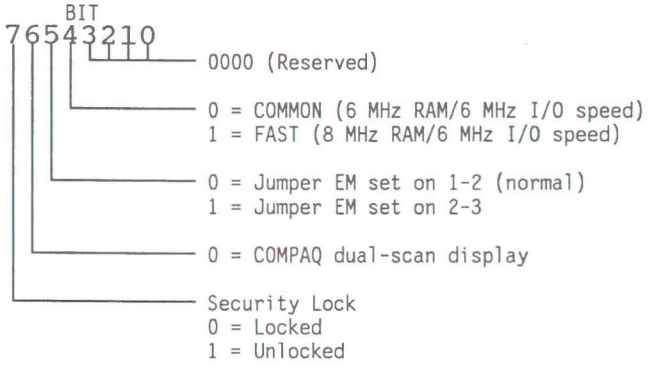


Figure 2-14. 8042 Input Port - Bit Definition

To read the 8042 TEST input port value:

1. Write the command E0h (transfer the current TEST input port values to the 8042 output buffer) to I/O address 64h.
2. Read the 8042 output buffer (port address 60h).

Figure 2-15 shows the format of the byte returned by the 8042 TEST input port.

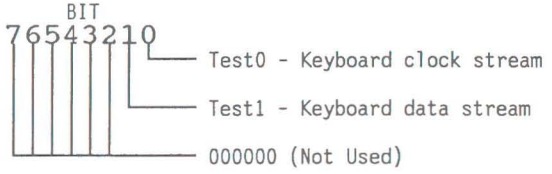


Figure 2-15. 8042 Test Input Port - Bit Definition

Programming the 8042

The 8042 is I/O-mapped at port addresses 60h and 64h.

Prior to writing a command or data to ports 60h or 64h, the 8042 Status register must indicate "Input Buffer Empty". Also, prior to reading data from port 60h, test the 8042 Status register to ensure a "Data in Buffer" condition.

Port 60h, Data I/O Register. Use the 80286's IN instruction to read data from the 8042's output buffer. Data in the Data I/O register is from the keyboard, unless the 8042 has been given a command such as 20h, Read Command byte.

Use the 80286's OUT instruction to send data to the keyboard, unless the 8042 has been given a multibyte command such as 60h, Write Command Byte. To give a multibyte command to the keyboard, write the first command byte to port 64h and the second command byte to 60h.

Port 64h, Command/Status Register. The following pages describe the format for Command/Status register (port 64h) I/O interactions with the 8042.

Use the 80286's IN instruction to read the status of the 8042 and the keyboard (input from port 64h).

Use the 80286's OUT instruction to give a command to the 8042 (output to port 64h). Writing to this address automatically sets the COMMAND/DATA flag to 1.

Most commands involve a single write step. However, some commands do require a second step, such as a subsequent 8042 register read or write.

Figure 2-16 shows the 8042 Status register. Figure 2-17 shows the 8042 command byte. Table 2-12 lists the 8042 command codes.

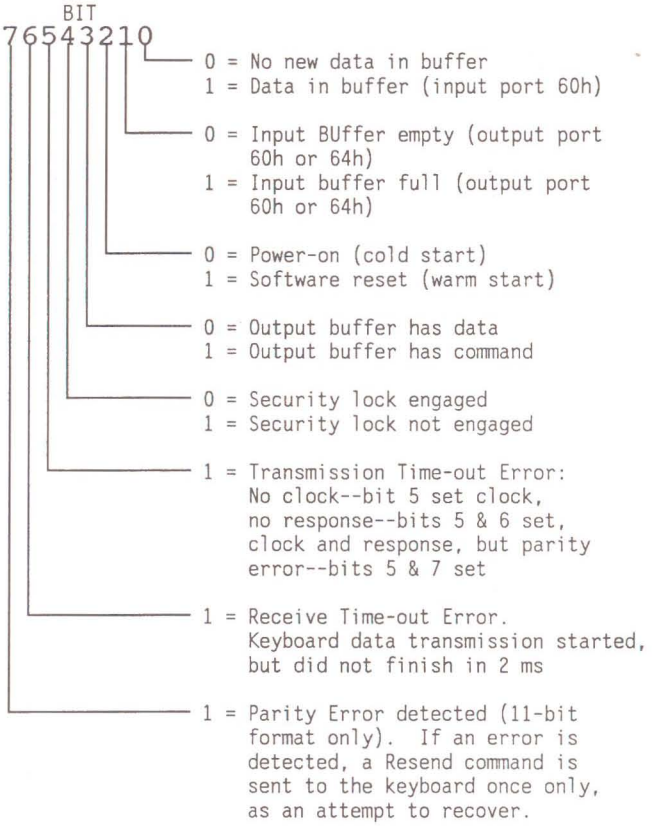


Figure 2-16. 8042 Status Register (Input Port 64h)

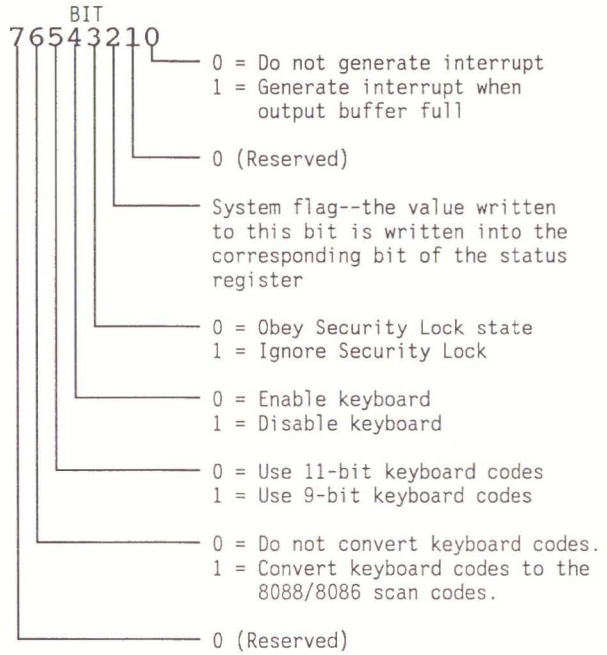


Figure 2-17. 8042 Command Byte (Output Port 64h).

Table 2-12. 8042 Command Codes (Output Port 64)

Code	Function
20h	Put the current command byte on the 8042's output port
60h	Load the next byte put into the 8042's input port as the command byte
A1h	COMMON Speed--the 8042 output port selects the 6-MHz RAM/6-MHz I/O speed (SLOWDOWN bit = 0 , SPEEDUP bit = 1.)
A2h	FAST Speed--the 8042 output port selects an address-dependent speed (SLOWDOWN bit and SPEEDUP bit = 1.)
A3h	HIGH Speed--the 8042 output port selects the 8-MHz RAM/8-MHz I/O speed (SLOWDOWN bit = 1 , SPEEDUP bit = 0.)
A4h	Toggle--the 8042 changes its speed-control output port bits between the COMMON mode speed and the speed defined with the HIGHSP command (A6h).
A5h	Special Read--the 8042 places the real value of port 2 except for bits 4 and 5 which are given a new definition in the output buffer. No output-buffer full is generated. If bit 5 = 0 then a 9-bit keyboard is in use If bit 5 = 1, then an 11-bit keyboard is in use If bit 4 = 0, the interrupt is disabled If bit 4 = 1, when the output buffer full interrupt is enabled
A6h	HIGHSP--the 8042 interprets the next byte written to port 60h as the maximum speed for the system when the Toggle command (A4h) is used. Value — Highest Speed 00h — COMMON (6 MHz RAM/6 MHz I/O speed) 01h — FAST (address-dependent 8 MHz RAM/6 MHz I/O speed) 02h — HIGH (8 MHz RAM/8 MHz I/O speed) Note: Only the two least-significant bits are used. The other bits should be set to 0.

(Continued)

Table 2-12. (Continued)

Code	Function
AAh	Initialization--the 8042 initializes ports 1 and 2 to their setup value, sets HIGHSP (CPU speed) to the value set by the jumper, disables the keyboard and clears the buffer pointers. It then places 55h in the output buffer.
ABh	Interface Test--directs the 8042 to test the data and clock lines of the keyboard interface. The output buffer (input port 60h) receives the test results, according to: 00h - No error detected 01h - The keyboard clock line is stuck low 02h - The keyboard clock line is stuck high 03h - The keyboard data line is stuck low 04h - The keyboard data line is stuck high 05h - COMPAQ diagnostic feature Note: The keyboard data line test does not check for line stuck low for 9-bit keyboards.
ACh	Diagnostic Dump--Reserved for diagnostic purposes.
ADh	Disable Keyboard--sets bit 4 of the 8042's command byte, which disables the keyboard interface. Data is not sent or received until the keyboard is enabled.
AEh	Enable Keyboard--resets bit 4 of the 8042's command byte, which enables the keyboard interface.
C0h	Read Input Port--directs the 8042 to transfer the status of the input port and place it in the output buffer (input port 60h). Use this command only when the output buffer is empty.
D0h	Read Output Port--directs the 8042 to transfer the current byte in the output port to the output buffer (input port 60h). The values for the SPEEDUP and SLOWDOWN bits (D6 & D7) will not be accurate. Use the Special Read command (A5h) to read the correct values. Use the Read Output Port command only when the output buffer is empty.

(Continued)

Table 2-12. (Continued)

Code	Function
D1h	Write Output Port--place the next byte written to the 8042 data register (output port 60h) on the 8042's output port. The system speed bits are not set by this command--use commands A1h to A6h for speed functions.

CAUTION

Setting bit 0 of the 8042's Output Port 0 puts the system in a reset state until the power is turned off.

E0h	Read Test0 and Test1 Inputs--directs the 8042 to put the current state of Test0 and Test1 into the output buffer (output port 60h). Test0 is bit 0 and Test1 is bit 1.
F0h-FFh	Pulse Output Port--the 8042's output port, bits <3..0>, can be pulsed (strobed low) for approximately 2 us. Bits <3..0> of this command byte each represent one bit, or signal of the output port to be pulsed. Note: Bit 0 of the 8042's Output Port 0 is connected to the system reset. Pulsing bit 0 will reset the system.

System Scan Codes

Table 2-13 shows the codes sent by the keyboard to the 8042 for each key, and the final code sent to the system by the 8042.

Table 2-13. Keyboard Scan Codes

US Character	11-bit Keyboard Scan Code	System Scan Code	9-Bit Keyboard Scan Code
	00h	FFh (Note 1)	
ESC	76h	01h	01h
1,!	16h	02h	02h
2,@	1Eh	03h	03h
3,#	26h	04h	04h
4,$	25h	05h	05h
5,%	2Eh	06h	06h
6,^	36h	07h	07h
7,&	3Dh	08h	08h
8,*	3Eh	09h	09h
9,(	46h	0Ah	0Ah
0,)	45h	0Bh	0Bh
-,_	4Eh	0Ch	0Ch
=,+	55h	0Dh	0Dh
<--	66h	0Eh	0Eh

(Continued)

Table 2-13. (Continued)

US Character	11-bit Keyboard Scan Code	System Scan Code	9-Bit Keyboard Scan Code
Tab	0Dh	0Fh	0Fh
Q	15h	10h	10h
W	1Dh	11h	11h
E	24h	12h	12h
R	2Dh	13h	13h
T	2Ch	14h	14h
Y	35h	15h	15h
U	3Ch	16h	16h
I	43h	17h	17h
O	44h	18h	18h
P	4Dh	19h	19h
[,{	54h	1Ah	1Ah
],}	5Bh	1Bh	1Bh
RET	5Ah	1Ch	1Ch
Ctrl	14h	1Dh	1Dh
A	1Ch	1Eh	1Eh
S	1Bh	1Fh	1Fh
D	23h	20h	20h
F	2Bh	21h	21h
G	34h	22h	22h

(Continued)

Table 2-13. (Continued)

US Character	11-bit Keyboard Scan Code	System Scan Code	9-Bit Keyboard Scan Code
H	33h	23h	23h
J	3Bh	24h	24h
K	42h	25h	25h
L	4Bh	26h	26h
;,:	4Ch	27h	27h
',"	52h	28h	28h
`,~	0Eh	29h	29h
Lshift	12h	2Ah	2Ah
\,|	5Dh	2Bh	2Bh
Z	1Ah	2Ch	2Ch
X	22h	2Dh	2Dh
C	21h	2Eh	2Eh
V	2Ah	2Fh	2Fh
B	32h	30h	30h
N	31h	31h	31h
M	3Ah	32h	32h
,,<	41h	33h	33h
.,>	49h	34h	34h
/,?	4Ah	35h	35h
Rshift	59h	36h	36h
*,PrtSc	7Ch	37h	37h

(Continued)

Table 2-13. (Continued)

US Character	11-bit Keyboard Scan Code	System Scan Code	9-Bit Keyboard Scan Code
Alt	11h	38h	38h
Space	29h	39h	39h
Caps Lock	58h	3Ah	3Ah
F1	05h	3Bh	3Bh
F2	06h	3Ch	3Ch
F3	04h	3Dh	3Dh
F4	0Ch	3Eh	3Eh
F5	03h	3Fh	3Fh
F6	0Bh	40h	40h
F7	02h,83h (Note 2)	41h	41h
F8	0Ah	42h	42h
F9	01h	43h	43h
F10	09h	44h	44h
Num Lock	77h	45h	45h
Scroll Lock	7Eh	46h	46h
Home,7	6Ch	47h	47h
Up,8	75h	48h	48h
PgUp,9	7Dh	49h	49h

(Continued)

Table 2-13. (Continued)

US Character	11-bit Keyboard Scan Code	System Scan Code	9-Bit Keyboard Scan Code
-	7Bh	4Ah	4Ah
Left,4	6Bh	4Bh	4Bh
5	73h	4Ch	4Ch
Right,6	74h	4Dh	4Dh
+	79h	4Eh	4Eh
End,1	69h	4Fh	4Fh
Down,2	72h	50h	50h
PgDn,3	7Ah	51h	51h
Ins,0	70h	52h	52h
Del,.	71h	53h	53h
Sys Req	7Fh,84h (Note 2)	54h	

(Continued)

Table 2-13. (Continued)

US Character	11-Bit Keyboard Scan Code	System Scan Code	9-Bit Keyboard Scan Code
R (Note 3)	60h	55h	
R (Note 3)	61h	56h	
F11 (Note 4)	78h	57h	
F12 (Note 4)	07h	58h	
R (Note 3)		59h through 7Fh	

Notes: 1. When the 8042 cannot read data from the keyboard, the 8042 sends FFh to the system, and sets the parity error bit of the Status register.

2. The second value is generated when the 8042 translates a 9-bit code to an 11-bit code.
3. R = Reserved
4. The F11 and F12 keys (System Scan Codes 57H and 58h respectively) are only available on the COMPAQ Enhanced Keyboard.

8042/Keyboard Communications Time Restraints

If a code transmission from the keyboard exceeds 2 ms, a time-out error results and the 8042 sends FFh to the system. No retries are attempted from a time-out error.

A keyboard clock signal strobes the 8042 during a data transmission to cycle data bits from the 8042 to the keyboard.

If the keyboard clock does not begin strobing within 15 ms after a byte is ready to transmit, or if the byte is not completely transmitted within 2 ms, the 8042 sends FEh to the system and sets the transmit time-out error bit in the status register.

The keyboard must respond to all transmissions from the 8042 within 25 ms, or the parity and time-out error bits are set in the status register of the 8042 and FEh is sent to the system. No retries are attempted by the 8042 after any data transmission error.

Security Key Lock

The security key lock is connected to the P17 line of the 8042 keyboard processor. When the security lock is unlocked, the keyboard is disabled. This feature allows a program to continue without accidental interference.

Interval Timer

The purpose of a programmable interval timer is to generate pulses at software-controllable intervals.

An Intel 8254 Programmable Interval Counter on the system boards provide three frequencies, or timed pulses for the system. The three counters count down a 16-bit value at a rate of 1.193 million counts-per-second and give an output pulse on the OUT pins. Table 2-14 lists the interval timer functions.

Two channels (interrupt and refresh) are on at all times; only the speaker tone can be disabled and enabled.

Table 2-14. Interval Timer Functions

Function	Counter 0 System Timer
Gate	Always On
Clock In	1.193 MHz
Clock Out	8259A IRQ0
Function	Counter 1 Refresh Request
Gate	Always On
Clock In	1.193 MHz
Clock Out	Request Refresh
Function	Counter 2 Speaker Tone
Gate	Programmable
Clock In	1.193 MHz
Clock Out	Speaker Input

Interval Timer Architecture

The interval timer contains three identical counters. Figure 2-18 shows the architecture of the interval timer. CRm and CRl contain the most- and least-significant bytes of the 16-bit initial count value. These registers are cleared when they are both transferred into CE.

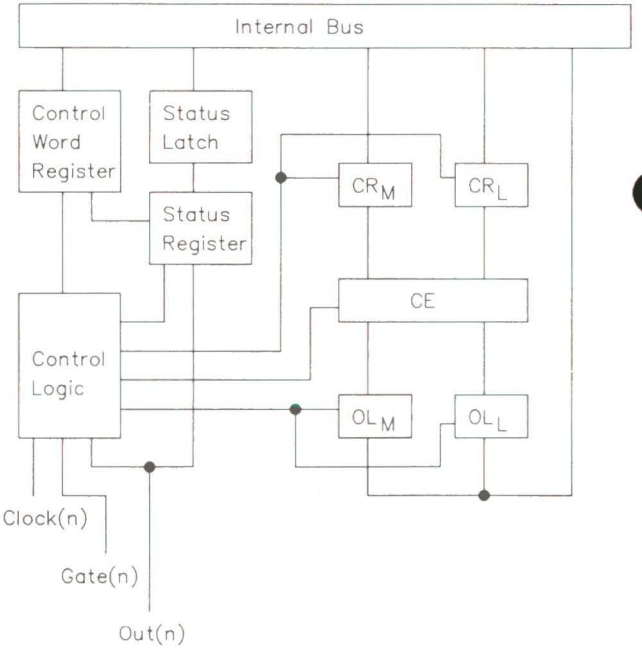


Figure 2-18. Counter Architecture

CE is the actual "Counting Element" latch that contains the value being counted down.

OLm and OLl contain the most- and least-significant bytes of the CE value, unless a latch command is given. In this case, the OLm and OLl registers hold the count until read.

Programming the Interval Timer

The timer is an I/O-mapped device. Table 2-15 lists the ports used. Several commands are available:

- The Control Word specifies:
  - which counter to read or write
  - the operating mode
  - the count format
- The Counter-Latch command latches the current count so that it can be read by the system. The count-down process continues.
- The Read-Back command reads the count value, programmed mode, the current state of the OUT pins, and the state of the Null Count Flag of the selected counter.

Table 2-15. Interval Timer Port Assignments

Port	Function
40h	Read or Write Count for Counter 0 (System Clock)
41h	Read or Write Count for Counter 1 (Refresh Request)
42h	Read or Write Count for Counter 2 (Speaker Tone)
43h	Input for Control Word, Counter Latch, or Read-Back commands (Command Mode Register)

Interval Timer Operating Modes and Initial Values

Six operating modes are available (See Table 2-16).

Table 2-16. Interval Timer Operating Modes

Mode	Function
0	Out signal on end-of-count (=0)
1	Hardware retriggerable one-shot
2	Rate generator (divide-by-n counter)
3	Square-wave output
4	Software-triggered strobe
5	Hardware-triggered strobe

The three counters are initialized with the values shown in Table 2-17.

Table 2-17. Interval Timer Initial Values

Counter	Mode	Control Word	Count	Frequency
0	3	36h	65535	18.207 Hz
1	2	54h (See Note)	19	62.799 KHz
2	3	B6h	1336	893.10 Hz

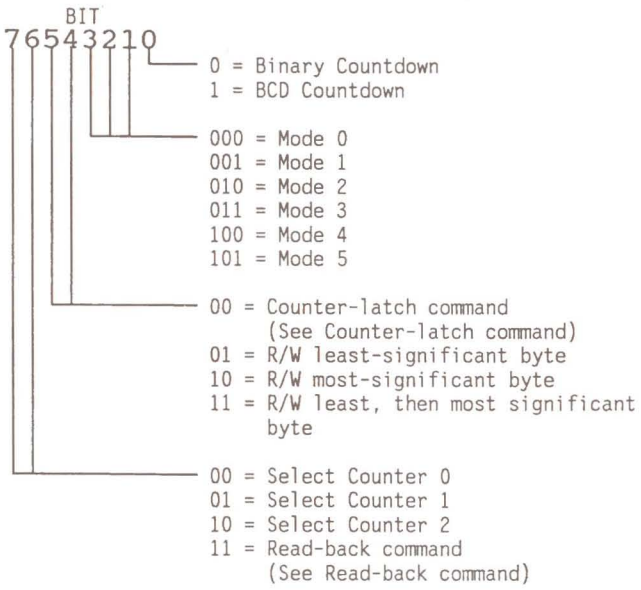
Note: Only the least-significant byte of the divisor is loaded.

Programming the interval timer is a simple process:

1. Write a control word.
2. Write an initial count for each counter.
3. Load the least- and most-significant bytes of the 16-bit counter in two steps (writes).

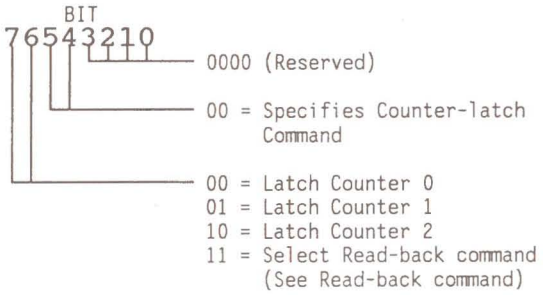
Interval Timer Control Word Format

The Control Word specifies the counter, whether it is to be written to or read from, the operating mode, and whether it counts down in a 16-bit or binary-coded decimal (BCD) format.



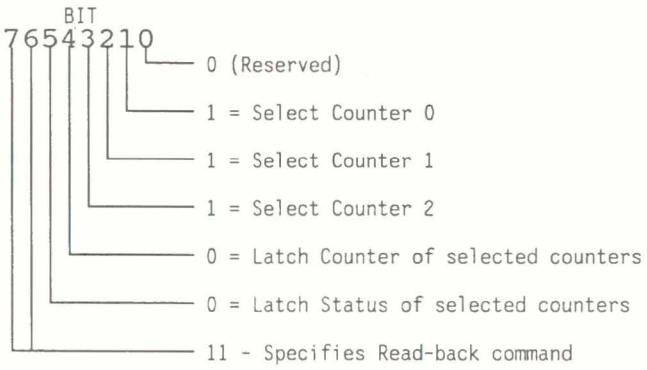
Interval Timer Counter-latch Command

The Counter-latch command latches the count at the time the command is received. The count is held in the OL registers until read.

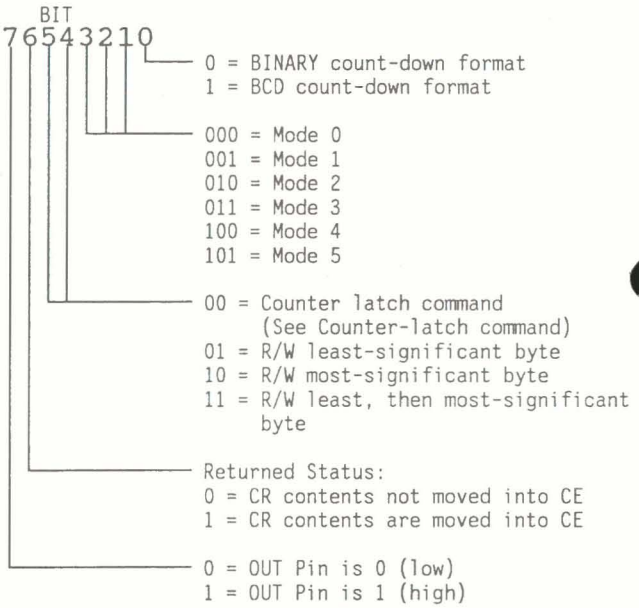


Interval Timer Read-back Command

The Read-back command causes the count or status of the counters to be latched in the OL registers until read. A single read-back can latch the count or status of all three counters.



The status byte latched into OL has the format:



Interrupt Priority Encoders

The 80286 processor has two signals for interrupts, labelled NMI (nonmaskable interrupt) and INTR (maskable interrupts). A maskable interrupt is an interrupt that can be enabled or disabled by the processor STI/CLI instructions. A nonmaskable interrupt is not masked off by the CLI instruction but can be disabled under software control by the system board logic.

NMI Interrupt Facts

NMI interrupts are caused by parity errors on the system board, memory boards, or any expansion boards which pull the IOCHK- line low.

System software can also generate a software interrupt to the NMI routine. When the IOCHK- line is pulled low, it sets the IOCHK- latch, which holds the error condition until software can examine it.

The source of the NMI can be determined by examining input port 61h, bit 6. If this bit is set, the interrupt came from the hardware IOCHK- line. To clear the hardware IOCHK- latch, pulse bit 3 of port 61h high.

The mask register for the NMI interrupt is at I/O-address 70h. The format for this byte is 10000000, that is, only the most significant bit is decoded. Write an 80h to port 70h to mask the NMI signal. This port is shared with the Real-Time Clock and Configuration Memory Device (the lower 6 bits). Do not modify the contents of this register without considering the effects on the state of the other bits.

INTR Interrupt Facts

All INTR-type interrupts to the CPU are channeled through the interrupt controllers (8259A). These devices generate interrupts on the 80286's interrupt line, which can be masked in the 80286 by software.

The interrupt controllers are 8-input devices that can accept interrupt signals from several devices, then prioritize them and interrupt the processor. The processor then automatically reads the interrupt controller to determine the source of the highest-priority interrupt and calls the appropriate interrupt routine.

Two interrupt controllers (a master and a slave) are used so that more than eight levels of interrupt are possible. The slave (Interrupt Controller 2) interrupts the master (Interrupt Controller 1) to show an interrupt. When Interrupt Controller 1 is properly programmed (in the special fully nested mode) Interrupt Controller 2 sends the correct interrupt vector to the CPU for the source of the interrupt. Figure 2-19 shows a diagram of the interrupt controller circuit.

All interrupts can be masked off, using the CLI instruction of the 80286. The base I/O address for Interrupt Controller 1 is 20h; for Interrupt Controller 2 it is A0h. Table 2-18 lists the initial interrupt controller values.

Table 2-18. Initial Interrupt Controller Values

Port	Value	Description of Contents
20h	11h	Cntlr 1, ICW1
21h	08h	Cntlr 1, ICW2 vector address for 000020h
21h	04h	Cntlr 1, ICW3 indicates slave connection
21h	01h	Cntlr 1, ICW4 8086 mode
A0h	11h	Cntlr 2, ICW1
A1h	70h	Cntlr 2, ICW2 vector address for 0001C0h
A1h	02h	Cntlr 2, ICW3 indicates slave ID
A1h	01h	Cntlr 2, ICW4 8086 mode
A21h	B8h	Cntlr 1, Interrupt mask (may vary with option)
A1h	9Dh	Cntlr 2, Interrupt mask (may vary with option)

Table 2-19 shows the 16 possible sources for an interrupt and their priorities. The highest-priority interrupt is processed first.

Table 2-19. Interrupts And Their Priorities

Priority	Label	Controller	Typical Interrupt Source
1	NMI	(Note)	Parity Error Detected
2	IRQ0	1	Interval Timer Output 0
3	IRQ1	1	Keyboard
	IRQ2	1	Interrupt from Controller 2
4	IRQ8	2	Real-Time Clock
5	IRQ9	2	Expansion Bus Pin B04
6	IRQ10	2	Expansion Bus Pin D03
7	IRQ11	2	Expansion Bus Pin D04
8	IRQ12	2	Expansion Bus Pin D05
9	IRQ13	2	Math Coprocessor
10	IRQ14	2	Fixed Disk Drive Controller --Expansion Bus Pin D07
11	IRQ15	2	Expansion Bus Pin D06
12	IRQ3	1	Serial Port 2 --Expansion Bus Pin B25
13	IRQ4	1	Serial Port 1 --Expansion Bus Pin B24
14	IRQ5	1	Parallel Port 2 --Expansion Bus Pin B23
15	IRQ6	1	Diskette Drive Controller --Expansion Bus Pin B22
16	IRQ7	1	Parallel Port 1 --Expansion Bus Pin B21

Note: The NMI signal is controlled through I/O port 70h, bit 7.

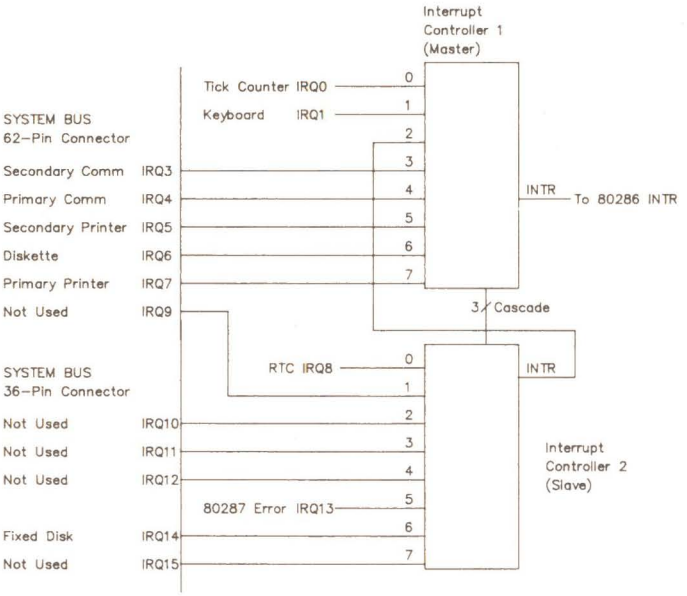


Figure 2-19. Interrupt Controller Circuit Diagram

2.5 EXPANSION BUS

The system board uses expansion slots to support additional circuit boards.

Expansion slots either have two connectors (62-pin and 36-pin) or one connector (62-pin). Slots with both connectors support a 16-bit data bus and the high-order address lines, LA<23..17> as well as additional interrupt and DMA lines. Slots with only one connector support only an 8-bit data bus with address lines SA<19..0>.

This section presents the expansion bus and the system timing requirements and includes:

- Detailed explanations of the expansion bus signals
- Major functions supplied to the expansion bus, such as:
  - Address Handling
  - Data Handling
  - Non-CPU Operations
  - DMA Operations
  - Dynamic RAM Refresh
  - Other Bus Master Operations
- Timing Considerations

Address Handling

When the CPU begins a bus cycle, it places an address on the address bus. This address may be placed on the bus even while the previous cycle is still in progress. Since most devices expect to see a valid address for the duration of a bus cycle, the system board latches the address onto the system bus.

System bus lines that contain the latched address are SA<19..0>. These latches are of the fall-through type so that when the address latch enable signal (ALE) goes active, the address appears at the output. When ALE goes inactive, the addresses will stay on the outputs until the next bus cycle begins.

Some high speed devices overlap some operations (such as address decoding). To allow this, the system bus provides a set of address lines (LA<23..17>) that are not latched but which provide a greater setup time to do decoding. When the address changes, expansion bus devices may decode the high-order address lines and then latch them using BALE. This allows expansion bus devices to take advantage of addresses for the next bus cycle that may be placed on the bus before the current bus cycle is complete.

When other devices (such as DMA or other bus masters) take control of the system bus, the BALE line is held active for the entire duration of the operation. As a result, expansion bus devices annot use BALE to latch the high-order address lines. Therefore, LA<23...17> should be held stable for the entire duration of each bus cycle.

Data Handling

Data handling for these products is accomplished with two data buses. The first is the 8-bit bus which is compatible with previous products. It is provided by the SD<7..0> lines. External devices and memory that are limited to 8-bit transfers will use this bus and the control lines SMRDC-, SMWTC-, IORC-, and IOWC- to enable or latch data on the bus.

Devices that can transfer data 16 bits at a time must also use the SD<15..8> lines for data transfer. The lines SBHE- and SA0 are used to determine which byte(s) are desired. These devices tell the system board that they are 16-bit devices by setting the M16- or IO16- (as appropriate) when they are addressed. Table 2-105 shows the relationship between the three lines.

Table 2-20. M16-, IO16-, SA0, and SBHE- Signal Relationship

M16- or IO16-	SA0	SBHE-	Cycle Type
High	High	----	Odd byte transfer on lines SD<7..0>
High	Low	----	Even byte transfer on lines SD<7..0>
Low	High	High	Reserved
Low	High	Low	Odd byte transfer on lines SD<15..8>
Low	Low	High	Even byte transfer on lines SD<7..0>
Low	Low	Low	Even word transfer on lines SD<15..0>

Non-CPU Operations

The system board supports several operations that are not related to the processor chip itself. They are refresh, traditional direct memory access, and expansion bus master access. Refresh is provided to prevent loss of data in dynamic RAMs (DRAMs). The other operations are used by expansion bus devices that require access to memory or I/O without processor intervention.

The system board prioritizes the requests for each type of service according to the following rules:

- If the CPU is the bus master, it completes the current processor cycle. (This includes word operations to 8-bit memory, which execute as two single-byte operations).
- If the CPU has an instruction LOCKed, it will complete the instruction.
- There is an automatic LOCK between an interrupt acknowledge and the first bus write in the acknowledge sequence.
- In the 80286 protected-virtual mode, segment-descriptor operations are automatically LOCKed (six words are loaded at one time).
- Refresh and other DMA cycles are started on a first-come, first-served basis after the CPU releases the bus.
- If a refresh is in progress when a DMA cycle is requested, the DMA cycle will be run without allowing the CPU to regain control of the bus.
- If a direct memory cycle is in progress when a refresh is requested, the refresh cycle will be run without allowing the CPU to regain control of the bus.
- The DMA controller will hold the bus until all outstanding DMA requests are handled.
- If a DMA channel is programmed for demand or block transfer modes, the DMA controller will keep the bus for the entire time to complete the programmed operation.
- Wait states or 8-bit memory anywhere in the system can delay the time required to acknowledge a DMA request.

Because of the above conditions, peripheral designers must assume that the latency on any DMA request can be as high as 10-12 us in a typical system using only diskette operations. If more than one DMA device is operating at one time, the latency can be even greater. If a program uses a LOCK prefix before string instructions or uses block- or demand-mode DMA, then the latency could reach the millisecond range.

DMA Operations

The DMA controllers in the system operate as a separate subsystem from the main bus controller. They handle requests from the DMA peripherals, arbitrate between them, and then request access to the system address and control lines from the CPU.

There are two types of DMA: byte and word. One of the DMA controllers is connected to handle byte-DMA operations, the other, word-DMA operations. To simplify the arbitration between sources, the request line from the byte controller is connected to a DMA request line (DRQ4) on the word controller. The word DMA controller is programmed for cascade mode on channel 0 (to which DRQ4 is connected) so that it will not actually place an address on the bus when it acknowledges the byte controller's request.

Byte-DMA Operations

The DMA byte cycle begins when a peripheral sets a DRQ<3..0> line active. The DMA controller then arbitrates among any other pending requests and sets the hold request output active. This line (DRQ4) is connected to the word controller as discussed above which does its arbitration. The word controller then sets its hold request line active which is in turn synchronized and arbitrated by the hold arbitration logic discussed above.

When the system responds to the request with an acknowledge, the word DMA controller will respond with a DAK4, which acts as a hold acknowledge to the byte controller. The byte controller will, after synchronizing the acknowledge, place an address on the bus lines.

Logic drives the SBHE- line in the opposite sense of SA0 in order to satisfy 16 bit devices on the bus. When this is complete, the DMA controller drives the lines IORC-, IOWC-, MWTC-, and MRDC- according to the type of cycle being run. If SA0 is high and the addressed memory is 16-bit, logic routes the data between the low half and high half of the data bus. The data is moved from high to low on memory reads, and from low to high on memory writes.

Word-DMA Operations

Word-DMA operations are only possible between word memory (16 bit) and word peripherals. Also, the DMA cannot operate on an odd-address boundary, on either memory or I/O. The system latches the SA0 and SBHE- lines to enable 16-bit devices on the bus.

The DMA-word cycle begins when a peripheral sets a DRQ5-DRQ7 line active. The DMA controllers then arbitrate among any other pending requests and set the hold request output active.

When the system responds to the request, the word DMA controller will, after synchronizing the acknowledge, respond with a DAKx acknowledge to the peripheral. The DMA controller will place the address on the bus and then drive the control lines.

Dynamic RAM Refresh

The dynamic RAM refresh subsystem is designed to do a memory read cycle on each of 256 addresses in the memory space as addressed by SA<7..0>. The other address lines are in an undefined state during the RAM refresh time. The system can also be driven by an external source if another bus master has control.

The system consists of a timer (part of the 8254) that generates the refresh requests every 15.924 us, arbitration logic that arbitrates whether the refresh controller or the DMA subsystem gets control of the bus, a timing generator, and a refresh address counter. The refresh request rate of 62.799 kHz provides 128 refresh cycles in 2.038 ms or 256 cycles in 4.0765 ms.

If an external bus master wishes to take the bus for long periods of time, it must perform refresh or risk losing the contents of dynamic memory. The external bus master can do this by developing its own refresh request timer and internal arbitration.

When it is not otherwise driving the bus, but still has bus control, the bus master can generate a refresh cycle by pulling the REFRESH- line low with an open collector gate. When the MRDC- line goes inactive from the refresh cycle, the REFRESH- line should be released. The external bus master can then take full control.

Other Bus-Master Operations

This system allows other bus masters to take over the system buses and use the I/O peripherals and memory. This is accomplished by the bus master software programming an unused DMA channel for cascade operation. When this is complete, the bus master can request the bus by setting the appropriate DRQx (<7..5>, <3..0>) line active and waiting for a response.

When the system responds with DAKx, the bus master can pull the GRAB- line active (low), disabling the address, data, and control lines. The bus master should then wait one BCLK period before enabling its own buffers with valid address information and wait one more BCLK period before driving the control lines.

When the bus master is finished, it should release the GRAB- and DRQx lines to allow the CPU to continue operations. If the bus master keeps control of the bus for more than 15 us, then it must provide its own refresh timing and request logic to prevent loss of dynamic memory contents.

Bus Driving/Loading Information

The following information is provided to improve the probability that third-party controller boards will work with the standard COMPAQ boards and options.

On bus lines that can be driven by a controller board, the driver should be able to sink a minimum of 20 mA and source 10 mA at 0.5 Vdc and 2.4 Vdc respectively.

On bus lines that are driven in the low direction only (open collector), the driver should be able to sink 20 mA at 0.5 Vdc.

The load on any logic line from a single bus slot should not exceed -2.0 mA in the low state (at 0.5 Vdc) or 0.1 mA in the high state (at 2.7 Vdc).

The logic-high voltage at the expansion bus ranges from 2.0 Vdc to 5.5 Vdc. The logic low voltage at the expansion bus ranges from -1.2 Vdc to 0.8 Vdc.

Bus Timing Information

In the FAST mode, the system clock toggles between two frequencies (8 MHz or 6 MHz):

- According to address, in which case the new speed will occur during the BALE time
- According to bus size (when M16- changes state), in which case the new speed will occur in the first clock after BALE.

During these changes, the bus timings for the affected cycles will be somewhere between the actual 8 MHz and 6 MHz timings. Table 2-21 lists the important timing parameters for the expansion slots. This information assumes that the system clock is at a constant speed of either 8 MHz or 6 MHz.

NOTE: The expansion bus timing information is provided to aid in a general understanding of the system and is subject to change.

Table 2-21. Expansion Slot Timing Parameters

Address access time from SA<19..0> address lines, 16 bit bus read cycle.	
Access time 8 MHz	228 ns
Access time 6 MHz	332 ns
Address access time from SA<19..1> address lines, 8 bit bus read cycle.	
Access time 8 MHz	603 ns
Access time 6 MHz	832 ns
Address access time from SA0 address line, 8 bit bus read cycle.	
Access time 8 MHz	589 ns
Access time 6 MHz	818 ns
Access time from BALE active, 16 bit bus read cycle.	
Access time 8 MHz	232 ns
Access time 6 MHz	336 ns
MRDC- Access time, 16-bit bus read cycle.	
Access time 8 MHz	190 ns
Access time 6 MHz	273 ns
IORC- access time, 16-bit bus read cycle.	
Access time 8 MHz	127 ns
Access time 6 MHz	190 ns
MRDC-, IORC-, access time, 8-bit bus read cycle.	
Access time 8 MHz	502 ns
Access time 6 MHz	690 ns

(Continued)

Table 2-21. (Continued)

SMRDC- access time, 8-bit bus read cycle.	
Access time 8 MHz	484 ns
Access time 6 MHz	672 ns
CPU read data hold from MRDC-, IROC-, inactive, 8-bit bus cycle.	
Hold	1 ns
LAx address valid to 16-bit memory command setup.	
Setup 8 MHz	106 ns
Setup 6 MHz	169 ns
16-bit bus memory cycle M16- low delay from LAx address valid.	
Maximum allowed delay 8 MHz	108 ns
Maximum allowed delay 6 MHz	171 ns
BALE valid to 16-bit memory command setup.	
Setup 8 MHz	20 ns
Setup 6 MHz	41 ns
BALE valid to M16- setup.	
Setup 8 MHz	7 ns
Setup 6 MHz	28 ns
SA<19..0> address valid to 16-bit memory command setup.	
Setup 8 MHz	22 ns
Setup 6 MHz	42 ns

(Continued)

Table 2-21. (Continued)

SA<19..0> address valid to I/O, 8-bit command setup.	
Setup 8 MHz	84 ns
Setup 6 MHz	126 ns
SA0 address hold from command.	
HOLD 8 MHz	96 ns
HOLD 6 MHz	137 ns
SA<19..1> address hold from command.	
HOLD 8 MHz	110 ns
HOLD 6 MHz	151 ns
CPU write data setup to MWTC- active, 16-bit bus memory cycle.	
Setup 8 MHz	-5 ns
Setup 6 MHz	+16 ns
CPU write data setup to IOWC- (16/8-bit), MWTC- (8-bit), active.	
Setup 8 MHz	58 ns
Setup 6 MHz	100 ns
CPU write data setup to MWTC-, IOWC-, inactive, 16-bit bus cycle.	
Setup 8 MHz	245 ns
Setup 6 MHz	350 ns

(Continued)

Table 2-21. (Continued)

CPU write data setup to MWTC-, IOWC-, inactive, 8-bit bus cycle.
Setup 8 MHz 620 ns
Setup 6 MHz 850 ns
Refresh address setup to MRDC- active
Setup 8 MHz 76 ns
Setup 6 MHz 118 ns
Refresh address hold from MRDC- inactive
HOLD -5 ns
Refresh wait state BUSRDY low delay from MRDC- active
Maximum allowed delay 8 MHz 90 ns
Maximum allowed delay 6 MHz 132 ns
Refresh wait state BUSRDY high setup to BCLK rising
Setup 5 ns
CPU memory or I/O command wait state BUSRDY high setup to BCLK rising
Setup 8 MHz 51 ns
CPU 16-bit memory command wait state BUSRDY low delay from command active
Maximum allowed delay 8 MHz 75 ns
Maximum allowed delay 6 MHz 117 ns

(Continued)

Table 2-21. (Continued)

CPU 16-bit I/O command wait state BUSRDY low delay from command active
Maximum allowed delay 8 MHz 12 ns
Maximum allowed delay 6 MHz 32 ns
CPU 8-bit command wait state BUSRDY low delay from command active
Maximum allowed delay 8 MHz 387 ns
Maximum allowed delay 6 MHz 532 ns
CPU minimum command active from BUSRDY high after added wait state.
Command active 8 MHz 135 ns
Command active 6 MHz 177 ns
CPU maximum command active from BUSRDY high after added wait state.
Command active 8 MHz 300 ns
Command active 6 MHz 382 ns
CPU 16-bit memory command no wait state NOWS- low delay from command active.
Maximum allowed delay 8 MHz 20 ns
Maximum allowed delay 6 MHz 41 ns
CPU 8-bit memory command no wait state NOWS- low setup to BLCK falling required.
Setup required 16 ns

(Continued)

Table 2-21. (Continued)

DMA memory read, I/O write command additional wait state. BUSRDY low delay from memory read command active.	
Maximum allowed delay 8 MHz	182 ns
Maximum allowed delay 6 MHz	265 ns
DMA I/O read, memory write command additional wait state. BUSRDY low delay from I/O read command active.	
Maximum allowed delay 8 MHz	273 ns
Maximum allowed delay 6 MHz	440 ns
Required I/O data access time from IORC- for DMA write to RAM.	
DMA I/O read access time 8 MHz	264 ns
DMA I/O read access time 6 MHz	347 ns
DATA valid after IOWC- low during DMA read from RAM.	
DMA data valid from IOWC- low	163 ns
DATA setup to IOWC- high during DMA read from RAM.	
Data setup to IOWC- high 8 MHz	217 ns
Data setup to IOWC- high 6 MHz	383 ns

2.6 MISCELLANEOUS SYSTEM BOARD INFORMATION

This section contains miscellaneous information that does not relate to any of the other sections, such as:

- Speed control
- Real-Time Clock and Configuration-Memory Battery
- Indicators
- Fuses
- Speaker Interface
- Clock Circuits
- System Board Power Requirements

Speed Control

The system boards have three speed modes:

- COMMON - I/O speed = 6 MHz, RAM speed = 6 MHz
- FAST - I/O speed = 6 MHz, RAM speed = 8 MHz
- HIGH - I/O speed = 8 MHz, RAM speed = 8 MHz

In the COMMON mode, all memory addresses or bus cycle types operate at 6 MHz except:

- DMA transfers (3 MHz (6 MHz/2)), and
- 80287 processes (4 MHz (12 MHz/3))

The FAST mode operates the system at a faster (8 MHz) speed except when this might cause a problem with operation of hardware options. In the FAST mode, the following memory addresses or bus cycle types continue to operate at 6 MHz:

- Memory with addresses 0A0000h to 0EFFFFh
- Memory with addresses FE0000h to FFFFFFh
- All I/O devices (except DMA transfers and 80287 processes)
- Any 8-bit memory device

In the FAST mode, the following memory addresses or bus cycle types operate at 8 MHz:

- RAM in base memory (000000h to 09FFFFh) unless it is 8-bit
- RAM in extended memory (100000h to FDFFFFh) unless it is 8-bit
- Standard ROM (0F0000h to 0FFFFFh)
- DMA transfers (half-speed (8 MHz/2))
- 80287 processes (5.33 MHz (16 MHz/3))

In the HIGH mode, all memory addresses or bus cycle types operate at 8 MHz except:

- 8 bit I/O or memory devices
- DMA transfers (half-speed (8 MHz/2)), and
- 80287 processes (5.33 MHz)

The speed is controlled by system software through the keyboard controller (8042).

The ES jumper located on the system board (switch 6 on the DESKPRO 286 with Version 2 System Board) sets the speed of the CPU when the system is powered up. When ES is in position 1-2, the CPU speed can be toggled between COMMON and FAST mode using the multiple key combination of Ctrl, Alt,\. When ES is in position 2-3, the CPU speed is limited to the COMMON mode and use of the multiple key combination Ctrl, Alt, \ will not affect the CPU speed.

The MODE SPE[ED] command overrides the ES setting in all cases.

NOTE: It is possible to restrict the CPU to the COMMON 6 MHz speed using the ES jumper.

Real-Time Clock and Configuration-Memory Battery

Table 2-22 lists the battery voltage range at the battery connector under load condition.

Table 2-22. Battery Connector Pinout

Pin	Function	Battery Voltage Min.	Max.
1	+5 Vdc Power	5.0	5.4
2	Keyed		
3	Not Used		
4	Ground	0.0	0.0

The voltage for a new battery must not exceed 6.2 V open circuit. The current drain on the battery varies with the voltage and the clock operating mode, but is between 50 to 90 ua after running SETUP. The maximum current is less than 150 uA.

CAUTION

Only COMPAQ Authorized Dealers should replace the system battery. Extreme caution must be observed to replace the battery with an identical battery type and on the correct connector pins.

Indicators (LEDs)

The COMPAQ PORTABLE 286 and COMPAQ DESKPRO 286 system boards have a light-emitting diode (LED) that lights when the +5 Vdc power is ON.

Fuses

The COMPAQ PORTABLE 286 system board and the COMPAQ DESKPRO 286 Version 2 system board have no user-replaceable fuses. The COMPAQ DESKPRO 286 Version 1 system board has two (Table 2-23).

Table 2-23. COMPAQ DESKPRO 286 Version 1 Fuses

F1, Keyboard Power Fuse, 2.5A
F2, Monitor Power Fuse, 2.5A

Speaker Interface

The speaker interface allows the speaker to be driven from two sources: the 8254-2 interval timer 2, or the processor through port 61h bit 1. In addition, the 8354 interval timer can be enabled and disabled from port 61h bit 0.

To use the 8254 interval timer to generate a tone, program Timer 2 to the desired frequency (the input clock rate is 1.193 MHz), and set port 61h bits 0 and 1 to 1. If the speaker is to be toggled directly by the CPU, port 61h bit 0 should be set to 0 and bit 1 should be toggled.

Clock Circuits

The two crystal oscillators on the system board provide:

- Clock frequencies for the 80286 processor and the entire system
- A clock source for video color burst signal and general timing

A crystal oscillator provides a 48-MHz frequency that is divided by 3 or 4 (software-selected) to provide the master clock for the clock-generator interface.

The clock generator interface further buffers the 12- or 16-MHz clock to supply the clocks used by the 80286, 80287, and other clocked devices. This interface also controls the reset signal. System reset does not occur until power levels are stable (PWRGOOD signal from power supply becomes active).

A second crystal oscillator on the system board provides a 14.31818-MHz (4 times 3.579545 MHz) clock signal for color-burst timing. This clock signal connects to pin B30 of the board slots for use by video controller and other boards.

System Board Power Requirements

Both system boards use +5 Vdc, and +12 Vdc power. They distribute power for other components of the system from the -5 Vdc, -12 Vdc and auxiliary +12 Vdc provided by the power supply.

2.7 GATE ARRAY DEVICES

The Version 2 system board of the COMPAQ DESKPRO 286 has three gate array devices:

- Memory and Speed Control (MSC) Gate Array
- Clock and Buffer Control (CBC) Gate Array
- Memory Map (MAP) Gate Array

The Gate Array Devices allow the size and cost of the system board to be reduced by consolidating the functions of several devices on the Type 1 system board. Both system boards are compatible, and are designed to the same programming standards.

This section describes the Gate Array Devices and provides a functional overview of each device.

MSC Gate Array

The MSC Gate Array includes the memory decoding and speed control functions resident on a Type 1 system board in (PALs) MEMCNT1, MEMCNT2, and SPEEDPAL.

The speed control function allows the selection of either an 8 MHz clock speed or a 6 MHz clock speed. The memory decoding functions include the generation of RAS-, CAS-, RAM-, MEM16, and ROM Enable- with multiple RAS and CAS lines for memory bank and hi/lo byte selection. In addition, the MSC Gate Array serves as a stand-alone memory controller for memory expansion boards.

CBC Gate Array

The CBC Gate Array incorporated the function of the 82284, 82288, and the CTRLPAL on the Version 1 system board. In addition, the CBC includes the clock switching/generation logic, generation of automatic and requested wait-states, shutdown logic, 8/16 bit bus conversion, and bus arbitration.

MAP Gate Array

The MAP Gate Array incorporates the functions of the Memory Page Register (74LS612), and PALs NCPPAL and PPIPAL on the Type 1 system board. In addition, the MAP Gate Array provides the circuitry for PORT B, SPEAKER and GATE control, REFRESH DETECT, and NMI control.

2.8 JUMPERS AND SWITCHES

The COMPAQ PORTABLE 286 and COMPAQ DESKPRO 286 Version 1 system boards have three jumpers in common. The ES jumper determines the CPU speed when power is applied and allows toggling of CPU through keyboard commands. The ED jumper indicates the primary display controller used when power is applied. EM is reserved for manufacturing test purposes. Table 2-24 defines the jumper settings.

Table 2-24. COMPAQ PORTABLE 286 and COMPAQ DESKPRO 286 Type 1 Common Jumpers

Label	Setting	Description
ES	2-3	CPU speed initial setting - 6MHz (COMMON)
	1-2	CPU speed toggle active (COMMON/FAST)
ED	2-3	COMPAQ Graphics or RGB video controller
	1-2	Non-COMPAQ monochrome/text video controller
EM	1-2	Reserved

The functions of the ES, ED, and EM jumpers are implemented with a switch on the COMPAQ DESKPRO 286 with Version 2 system board. Table 2-25 defines the switch settings.

Table 2-25. COMPAQ DESKPRO 286 (with Version 2 system board) Switch SW1 Settings

SW1 Position	Setting	Description
6	CLOSED	CPU speed initial setting - 6 MHz (COMMON)
	OPEN	CPU speed toggle active (COMMON/FAST)
	CLOSED	COMPAQ Graphics or RGBI Video Controller
8	OPEN	non-COMPAQ monochrome/text video controller
7	CLOSED	Reserved

Note: CLOSED = ON, OPEN = OFF

The COMPAQ PORTABLE 286 system board has several other jumpers which select the RAM and ROM configurations. These jumpers are explained in "The COMPAQ PORTABLE 286 Memory" section in this chapter. (See Chapter 4 for information on jumper settings when using a 512/2048 Kbyte Memory Expansion Board.).

The COMPAQ DESKPRO 286 (with Version 1 system board) RAM and ROM configuration jumpers are explained in Chapter 3, System Memory Board.

The COMPAQ DESKPRO 286 (with Version 2 system board) has jumpers which select the ROM type. The RAM configurations are controlled by switch settings (SW1, positions 1 through 5 on system board). These jumpers and switch settings are explained in "The COMPAQ DESKPRO 286 RAM" section in this chapter.

2.9 CONNECTORS

Tables 2-26 through 2-28 list the system board connectors. Table 2-29 describes the expansion slot signals. Figures 2-20 through 2-39 show the connectors on the system boards.

Table 2-26. System Board Connections

Function	COMPAQ PORTABLE 286	COMPAQ DESKPRO 286
DC power(In)	J116	J117
Drive power(Out)	J114-J115	J111-J112
Fixed disk drive power	J113	J109 or J110 (See Note)
Battery	J110	J118
Keyboard	J111	J116
Monitor power	J112	J113
Security lock	J117	J119
Speaker	J109	J115

Note: J110 is for an optional fixed disk drive back-up or second fixed disk drive.

Table 2-27. COMPAQ PORTABLE 286 System Board Expansion Slots

Slot	62-Pin	36-Pin	Function
1	J101	N/A	Diskette/Tape Controller
2	J102	N/A	Video Display Controller
3	J103	J106	Fixed Disk Drive Controller
4	J104	J107	Expansion (available)
5	J105	See Note	Expansion (available)

Note: Connector J108 is not installed.

Table 2-28. COMPAQ DESKPRO 286 System Board Expansion Slots

Slot	62-Pin	36-Pin	Function
1	J101	J121	Expansion (available)
2	J102	N/A	Expansion (available)
3	J103	J123	Expansion (available)
4	J104	J124	Expansion (available)
5	J105	J125	See Note
6	J106	J126	Fixed Disk Drive Controller
7	J107	J127	Video Display Controller
8	J108	N/A	Diskette/Tape Controller

Note: In the COMPAQ DESKPRO 286 with Version 1 system board, slot 5 contains the System Memory Board. In the COMPAQ DESKPRO 286 with Version 2 system board, slot 5 is available for expansion.

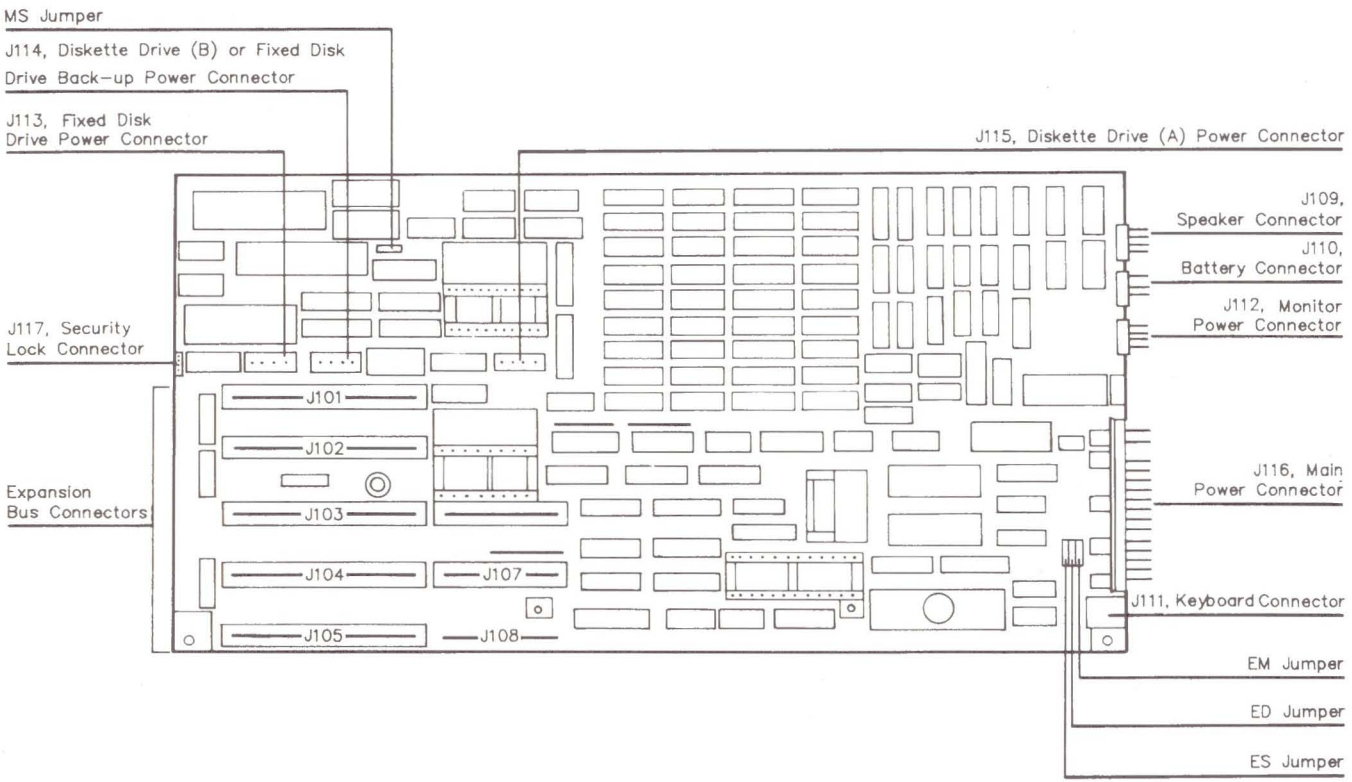


Figure 2-20. COMPAQ PORTABLE 286 System Board Connectors and Jumpers

Table 2-29. Expansion Slot Signals

Signal Name	Slot Pin	Type	Description
AEN	A11	O	This output signal when inactive (low) indicates that the CPU or controller board bus master has control of the bus. When active, the DMA controller has control of the bus. It is often used to disable devices which must not respond during a DMA cycle.
BALE	B28	O	This output signal (when high) indicates that a valid address is present on the LA<23..17> address lines. The LA<23..17> address lines or any decodes developed from them should be latched at the falling edge of BALE. This line is high when a DMA or bus master operation is occurring.
BCLK	B20	O	This output signal is provided to allow synchronization to the main processor clock. Its frequency will be either 6 MHz or 8 MHz with a duty cycle of 50%.
BUSRDY	A10	I	This input signal is used to lengthen a bus cycle from its standard time if a controller board cannot respond quickly enough. It should be pulled low by an open collector type device as soon as a slow addressed device is selected and held low until the device has responded. Bus cycles are lengthened by an integral number of (BCLK) cycles. This line should not be held low for more than 2.5 us. This line should be driven by an open-collector device capable of sinking 20 mA.
DAK0- DAK1- DAK2- DAK3- DAK5- DAK6- DAK7-	D08 B17 B26 B15 D10 D12 D14	O O O O O O O	These output lines (DMA Acknowledge) indicate that a request for a DMA service from the DMA subsystem has been recognized. The acknowledge is indicated by a LOW on this line. Use this line with the IORC- or IOWC- line to decode the desired DMA device. If used to signal acceptance of a bus-master request, this signal indicates when it is legal to pull GRAB- low.
DRQ0 DRQ1 DRQ2 DRQ3 DRQ5 DRQ6 DRQ7	D09 B18 B06 B16 D11 D13 D15	I I I I I I I	These input lines are used to request a DMA service from the DMA subsystem or to gain control of the system bus from the main CPU (DMA request). The request is made when the line goes from a low to a high and must remain high until the appropriate DAK<7..5>, <3..0> line goes active.

(Continued)

Table 2-29. (Continued)

Signal Name	Slot Pin	Type	Description
GRAB-	D17	I	This input signal is used to indicate that a controller board bus master is controlling the bus. A controller board can pull this line low when the appropriate DAK line is made active, signalling that a master request is granted. The system address, data and control lines will be floated, allowing the controller board to begin controlling them one full BCLK period after GRAB is made active. At least one more full BCLK period should be allowed after putting a valid address on the bus before activating any of the control lines. This line should be driven by an open-collector device capable of sinking 20 mA.
GROUND	B01 B10 B31 D18	-- -- -- --	These lines are connected to the system ac and dc ground. The maximum current allowed on any single contact is 1.5 A.
IOCHK-	A01	I	This input signal is used to signal the CPU about parity or other serious errors on controller boards. This signal should be driven low by an open collector type output capable of sinking 20 mA when an uncorrectable system error occurs.
IORC-	B14	I/O	This output line (I/O read) indicates (when low) when an I/O device is to send data to the data bus. It can be driven by a controller board acting as a bus master.
IOWC-	B13	I/O	This output line (I/O write) indicates (when low) when an I/O device is to accept the data from the data bus. It can be driven by a controller board acting as a bus master.
IO16-	D02	I	This input line (I/O is 16 bits) signals the system that the addressed I/O device is capable of transferring 16 bits of data at once. When this line is made active, during an I/O read or write, the standard one wait state I/O cycle will be run. This line should be driven low by an open-collector device capable of sinking 20 mA.
IRQ3 IRQ4 IRQ5 IRQ6 IRQ7 IRQ9 IRQ10 IRQ11 IRQ12 IRQ14 IRQ15	B25 B24 B23 B22 B21 B04 D03 D04 D05 D07 D06	I I I I I I I I I I I	These input lines are used to interrupt the CPU to request some service. The interrupt is recognized when the line goes from a low to a high and remains there until the appropriate interrupt service routine is executed.

(Continued)

Table 2-29. (Continued)

Signal Name	Slot Pin	Type	Description
LA17 LA18 LA19 LA20 LA21 LA22 LA23	C08 C07 C06 C05 C04 C03 C02	I/O I/O I/O I/O I/O I/O I/O	These output signals (Latchable Address) are used to decode memory which must respond with zero or one wait state. They are only guaranteed to be valid when BALE is high. These can be driven by a controller board acting as a bus master.
MRDC-	C09	I/O	This output line (Memory Read) indicates (when low) when a memory device is to send data to the data bus. This signal is active over the entire address space of the system. It can be driven by a controller board acting as a bus master.
MWTC-	C10	I/O	This output line (Memory Write) indicates (when low) when a memory device is to accept the data from the data bus. This signal is active over the entire address space of the system. It can be driven by a controller board acting as a bus master.
M16-	D01	I	This input line (memory is 16 bits) signals the system that the addressed memory is capable of transferring 16 bits of data at once. When this line is made active, during a memory read or write, the standard one wait state memory cycle will be run. This line should be derived from the LA<23..17> address lines. This line should be driven low by an open collector device capable of sinking 20 mA.
NOWS-	B08	I	This input line (No Wait State) is used to inform the system that standard wait states can be deleted for cycles when this line is made active. The line must be pulled low 45 ns before the falling edge of BCLK in order to be recognized. This line should be driven by an open-collector device capable of sinking 20 mA.
OSC	B30	O	This output signal is a clock for use in video color burst and other general timing applications. Its frequency is 14.31818 MHz and duty cycle is approximately 50%.
REFRESH-	B19	I/O	This output signal is used to indicate (when low) a refresh cycle in progress. It should be used to enable the SA<7..0> address lines to the row address inputs of all banks of dynamic memory so that when the MRDC- goes active, the entire system memory is refreshed at one time. It can be driven by a controller board acting as a bus master.
RESDRV	B02	O	This output signal is used to reset the hardware during powerup or power failure.

(Continued)

Table 2-29. (Continued)

Signal Name	Slot Pin	Type	Description
SA0	A31	I/O	These bidirectional signals address memory or I/O devices within the system. They form the low order 20 bits of the 24 bit address bits that the system offers. These lines are enabled onto the bus while BALE is high and are latched when BALE goes from a high to a low state. These can be driven by a controller board acting as a bus master.
SA1	A30	I/O	
SA2	A29	I/O	
SA3	A28	I/O	
SA4	A27	I/O	
SA5	A26	I/O	
SA6	A25	I/O	
SA7	A24	I/O	
SA8	A23	I/O	
SA9	A22	I/O	
SA10	A21	I/O	
SA11	A20	I/O	
SA12	A19	I/O	
SA13	A18	I/O	
SA14	A17	I/O	
SA15	A16	I/O	
SA16	A15	I/O	
SA17	A14	I/O	
SA18	A13	I/O	
SA19	A12	I/O	
SBHE-	C01	I/O	This output signal (System Bus High Enable) indicates (when low) that the high half of the SD data bus should transfer the data on boards which support the full 16-bit data bus. It can be driven by a controller board acting as a bus master.
SD0	A09	I/O	These bidirectional signals are the low 8 bits of the system data bus. They should be used exclusively by all eight bit devices to transfer data. Sixteen-bit devices should use these lines to transfer only the low half of a data word when the address line A0 is low. These can be driven by a controller board acting as a bus master.
SD1	A08	I/O	
SD2	A07	I/O	
SD3	A06	I/O	
SD4	A05	I/O	
SD5	A04	I/O	
SD6	A03	I/O	
SD7	A02	I/O	

(Continued)

Table 2-29. (Continued)

Signal Name	Slot Pin	Type	Description
SD08	C11	I/O	These bidirectional signals are the high 8 bits of the system data bus. Sixteen bit devices should use these lines to transfer the high half of a data word when the line SBHE- is low. These can be driven by a controller board acting as a bus master.
SD09	C12	I/O	
SD10	C13	I/O	
SD11	C14	I/O	
SD12	C15	I/O	
SD13	C16	I/O	
SD14	C17	I/O	
SD15	C18	I/O	
SMRDC-	B12	O	This output line (Standard Memory Read) is active (low) only when an address from 000000h to 0FFFFFh is decoded. This line is derived from MRDC-.
SMWTC-	B11	O	This output line (Standard Memory Write) is active (low) only when an address from 000000h to 0FFFFFh is decoded. This line is derived from MWTC-.
T/C	B27	O	This output signal (when high) indicates that the Terminal Count of a DMA operation has been reached. It should be decoded with the appropriate DAKx line for proper operation.
+5 Vdc	B03 B29 D16	-- -- --	These lines are connected to the system power supply for 5 volts. In addition to the maximum current available from the supply, the maximum current allowed on any single contact is 1.5 A.
-5 Vdc	B05	--	This line is connected to the system power supply for minus 5 volts. This supply is intended for low-current usage only (500 mA).
-12 Vdc	B07	--	This line is connected to the system power supply for minus 12 volts. This supply is intended for low-current usage only (1.0 A).
+12 Vdc	B09	--	This line is connected to the system power supply for 12 volts. In addition to the maximum current available from the supply, the maximum current allowed on this contact is 1.5 A.

The 36-pin connector conducts the high-order byte of the 16-bit data bus, the memory address lines for bits DAK<7..5>, LA<23..17>, signals, and more. These signals generally relate to 16-bit or high-address memory transfers.

The 62-pin connector conducts the signals needed by adapters that do not need word-length data transfers or access to more than the base 1 MB of memory.

Figure 2-21 shows the 36-pin connector and the signals that it provides.

Signal	Pin	Pin	Signal
M16–	D01	C01	SBHE–
IO16–	D02	C02	LA23
IRQ10	D03	C03	LA22
IRQ11	D04	C04	LA21
IRQ12	D05	C05	LA20
IRQ15	D06	C06	LA19
IRQ14	D07	C07	LA18
DACK0–	D08	C08	LA17
DRQ0	D09	C09	MRDC–
DACK5–	D10	C10	MWTC–
DRQ5	D11	C11	SD8
DACK6–	D12	C12	SD9
DRQ6	D13	C13	SD10
DACK7–	D14	C14	SD11
DRQ7	D15	C15	SD12
+5 V	D16	C16	SD13
GRAB–	D17	C17	SD14
SIGNAL GROUND	D18	C18	SD15

Figure 2-21. Expansion Slot - 36-Pin Connector

Figure 2-22 shows the 62-pin connector and the signals that it provides.

Signal	Pin	Pin	Signal
GROUND	B01	A01	IOCHK–
RESDRV	B02	A02	SD7
+5 Vdc	B03	A03	SD6
IRQ9	B04	A04	SD5
–5 Vdc	B05	A05	SD4
DRQ2	B06	A06	SD3
–12 Vdc	B07	A07	SD2
NOWS–	B08	A08	SD1
+12 Vdc	B09	A09	SD0
GROUND	B10	A10	BUSRDY
SMWTC–	B11	A11	AEN
SMRDC–	B12	A12	SA19
IOWC–	B13	A13	SA18
IORC–	B14	A14	SA17
DAK3–	B15	A15	SA16
DRQ3	B16	A16	SA15
DAK1–	B17	A17	SA14
DRQ1	B18	A18	SA13
REFRESH–	B19	A19	SA12
BCLK	B20	A20	SA11
IRQ7	B21	A21	SA10
IRQ6	B22	A22	SA9
IRQ5	B23	A23	SA8
IRQ4	B24	A24	SA7
IRQ3	B25	A25	SA6
DAK2–	B26	A26	SA5
T/C	B27	A27	SA4
BALE	B28	A28	SA3
+5 Vdc	B29	A29	SA2
OSC	B30	A30	SA1
SIGNAL GROUND	B31	A31	SA0

Figure 2-22. Expansion Slot - 62-Pin Connector

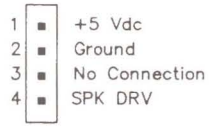


Figure 2-23. J109, COMPAQ PORTABLE 286 Speaker Connector

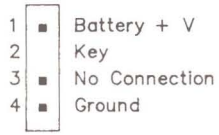


Figure 2-24. J110, COMPAQ PORTABLE 286 Battery Connector

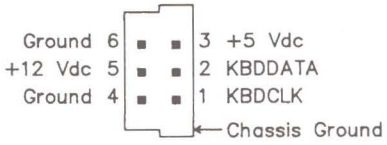


Figure 2-25. J111, COMPAQ PORTABLE 286 Keyboard Connector

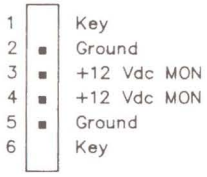


Figure 2-26. J112, COMPAQ PORTABLE 286 Monitor Connector

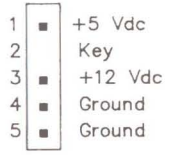
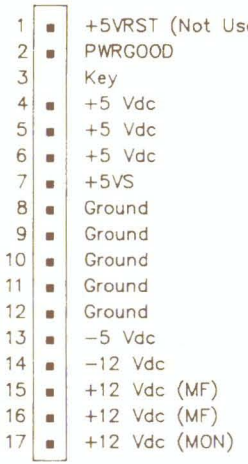


Figure 2-27. J113, J114, and J115, COMPAQ PORTABLE 286 Drive Power Connectors



Note: The maximum current for a single conductor (pin) must not exceed 5.0 A per line for +5 Vdc or 4.0 A for other lines.

Figure 2-28. J116, COMPAQ PORTABLE 286 Main Power Connector

Figure 2-29. J117, COMPAQ PORTABLE 286 Security Lock Connector

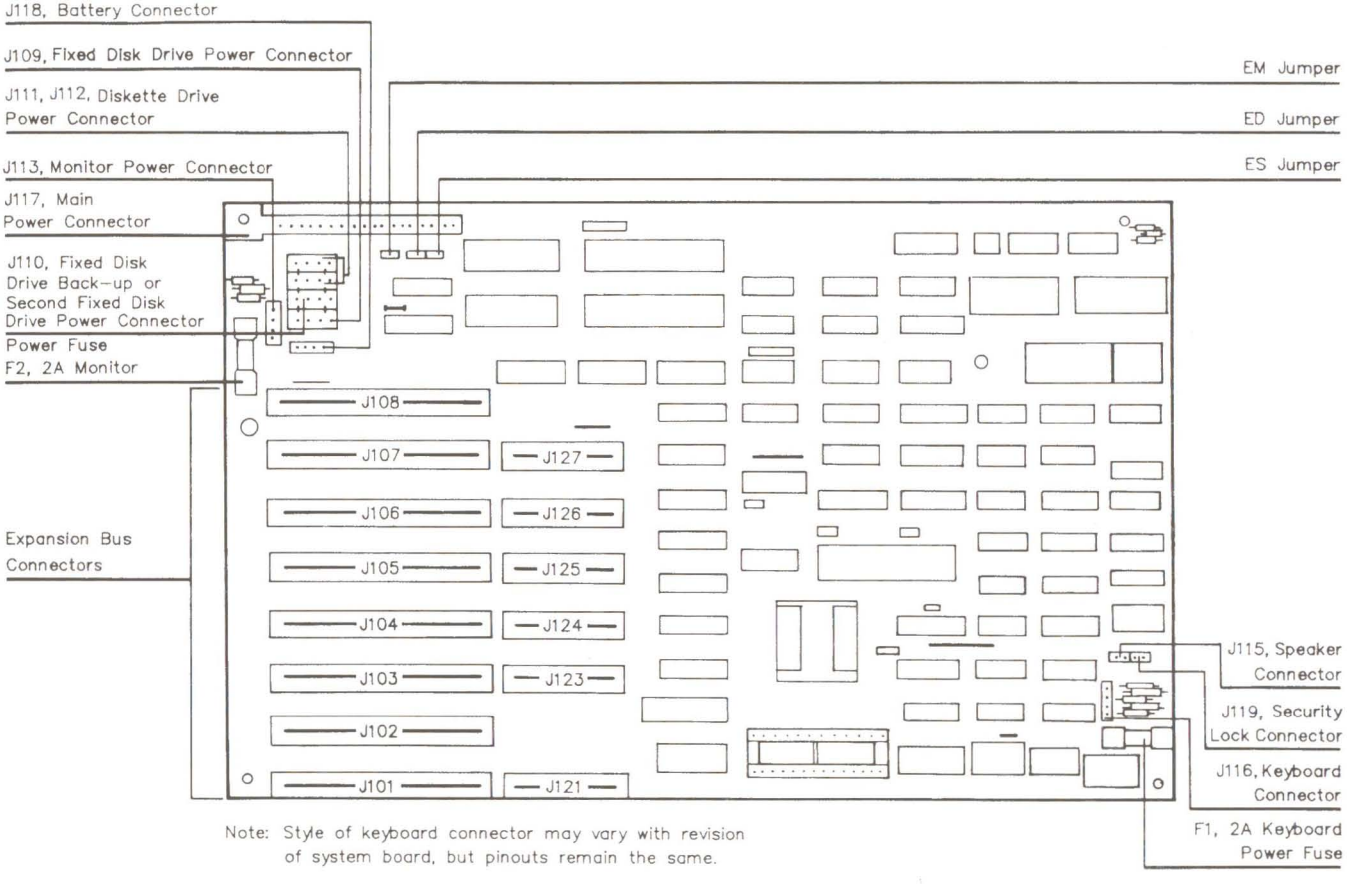


Figure 2-30. COMPAQ DESKPRO 286 Version 1 System Board Connectors and Jumpers

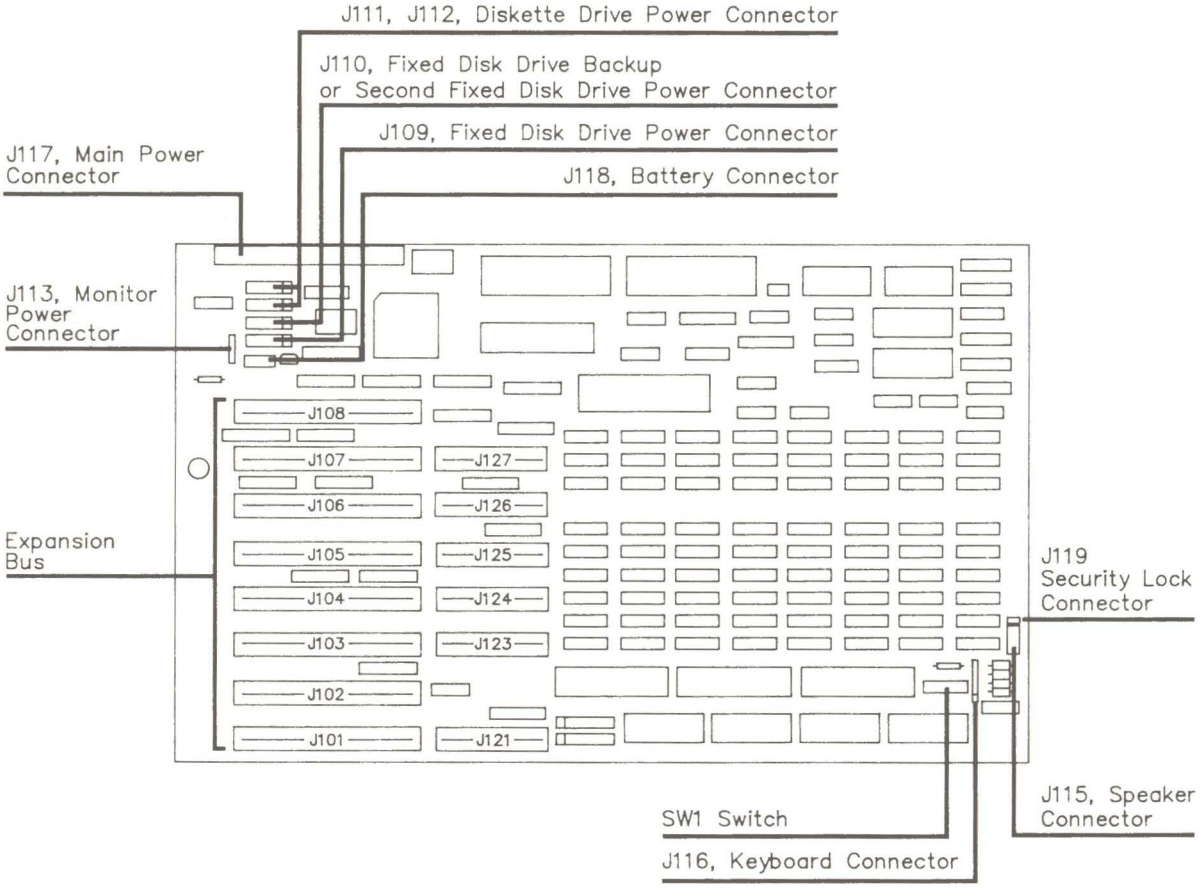


Figure 2-31. COMPAQ DESKPRO 286 Version 2 System Board Connectors and SW1 Location

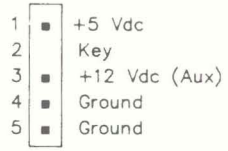


Figure 2-32. J109 and J110, COMPAQ DESKPRO 286 Fixed Disk Drive or Fixed Disk Drive Back-up Power Connector

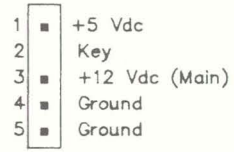


Figure 2-33. J111 and J112, COMPAQ DESKPRO 286 Diskette Drive Power Connectors

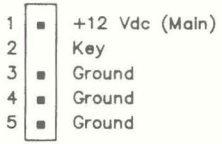
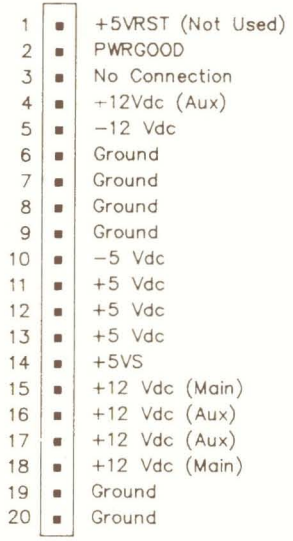


Figure 2-34. J113, COMPAQ DESKPRO 286 Monitor Power Connector

Figure 2-35. J115, COMPAQ DESKPRO 286 Speaker Connector

Figure 2-36. J116, COMPAQ DESKPRO 286 Keyboard Connector



Note: The maximum current for a single conductor (pin) must not exceed 5.0 A per line for +5 Vdc or 4.0 A for other lines.

Figure 2-37. J117, COMPAQ DESKPRO 286 Main Power Connector

Figure 2-38. J118, COMPAQ DESKPRO 286 Battery Connector

Figure 2-39. J119, COMPAQ DESKPRO 286 Security Lock Connector

2.10 COMPONENT LAYOUTS AND SCHEMATICS

Figure 2-40 shows the component layout for the COMPAQ PORTABLE 286 system board. Figure 2-41 shows the schematics for the COMPAQ PORTABLE 286 system board. Compaq Computer Corporation does not guarantee the accuracy of the component layout or the schematics. They are provided to aid in a general understanding of the system operation.

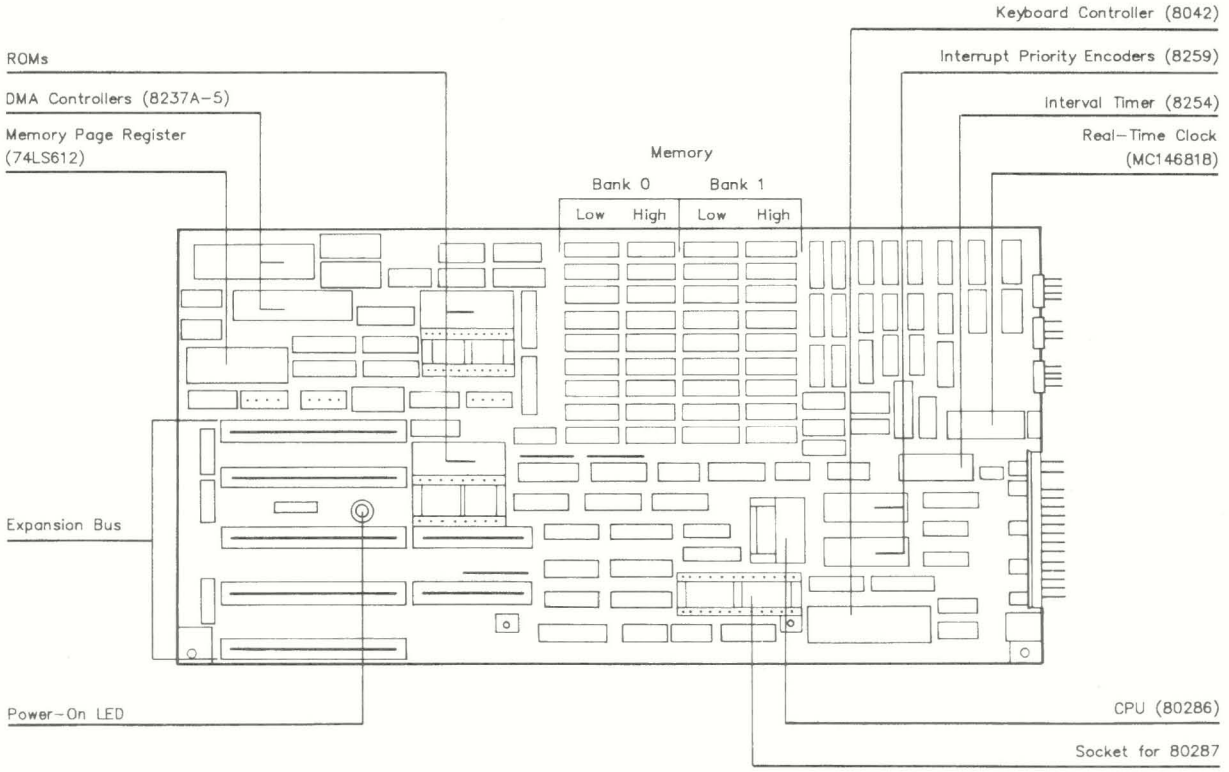


Figure 2-40. COMPAQ PORTABLE 286 System Board Component Layout (Page 1 of 1)

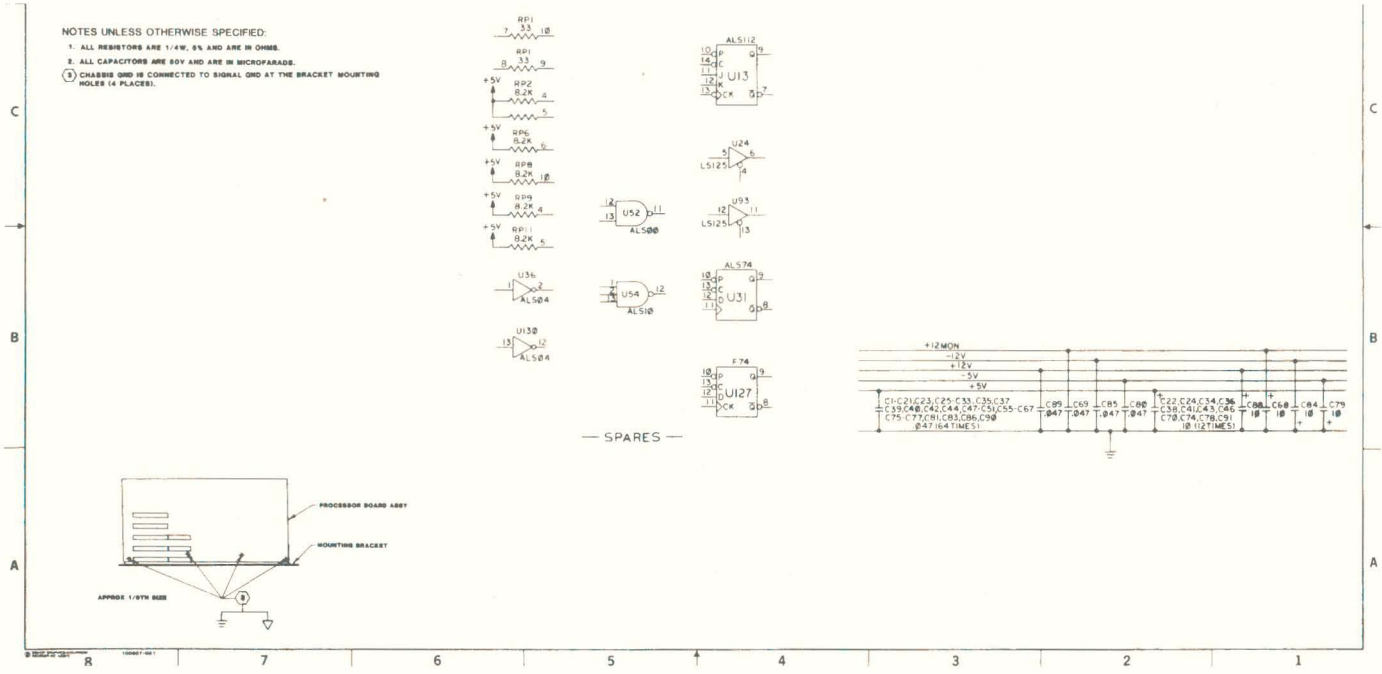


Figure 2-41. COMPAQ PORTABLE 286 System Board Schematics (Page 1 of 7)

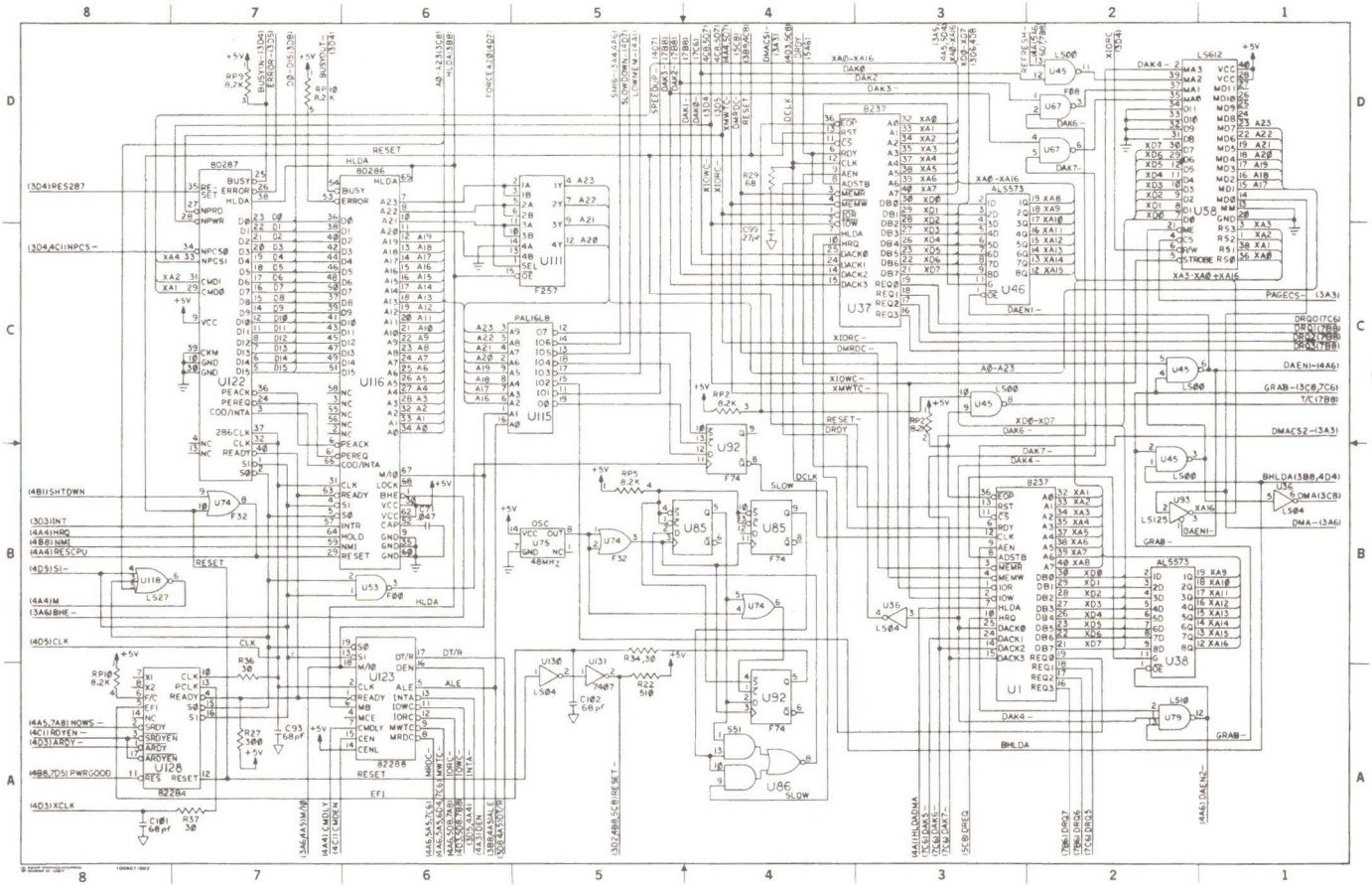


Figure 2-41. COMPAQ PORTABLE 286 System Board Schematics (Page 2 of 7)

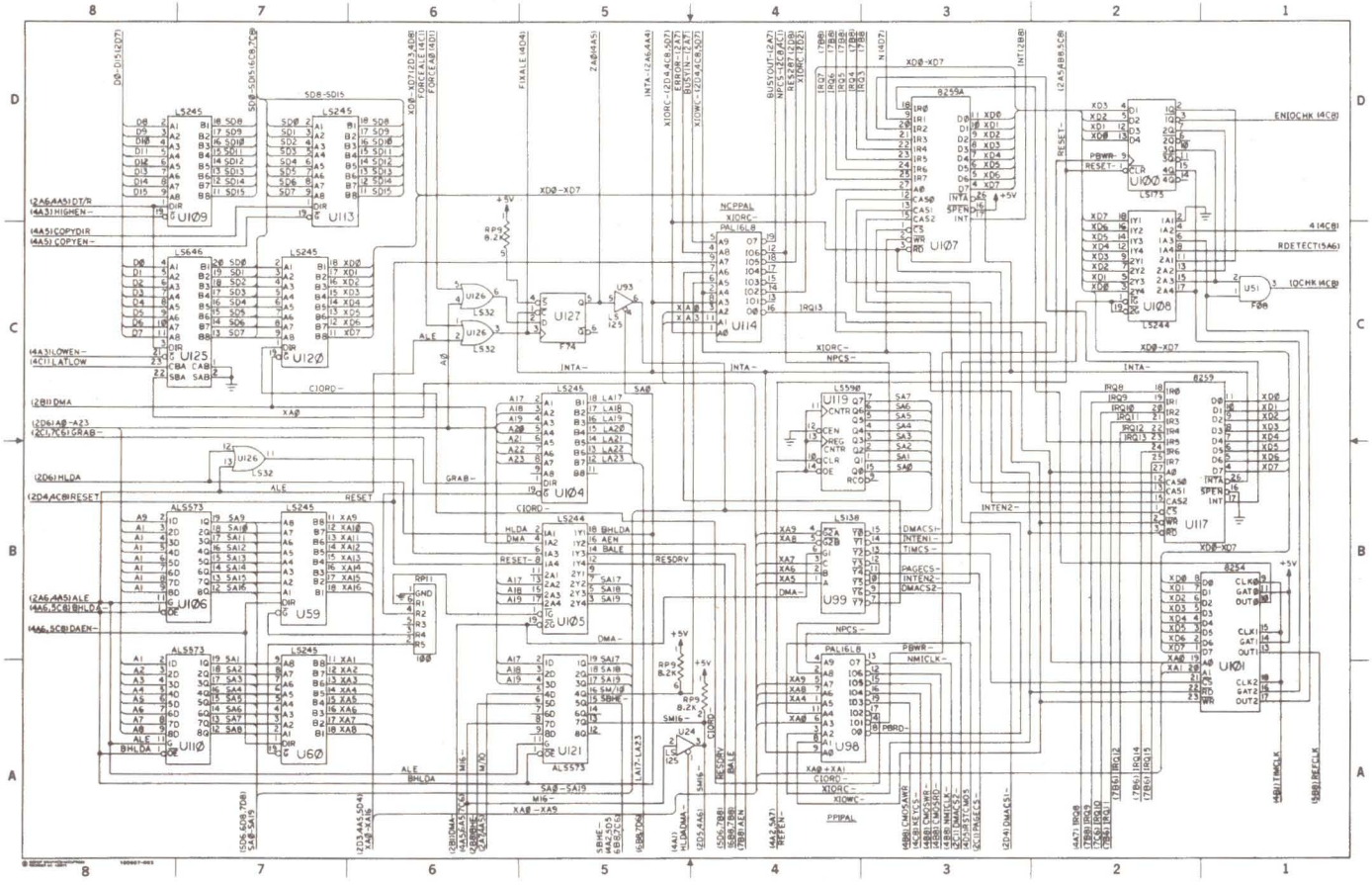


Figure 2-41. COMPAQ PORTABLE 286 System Board Schematics (Page 3 of 7)

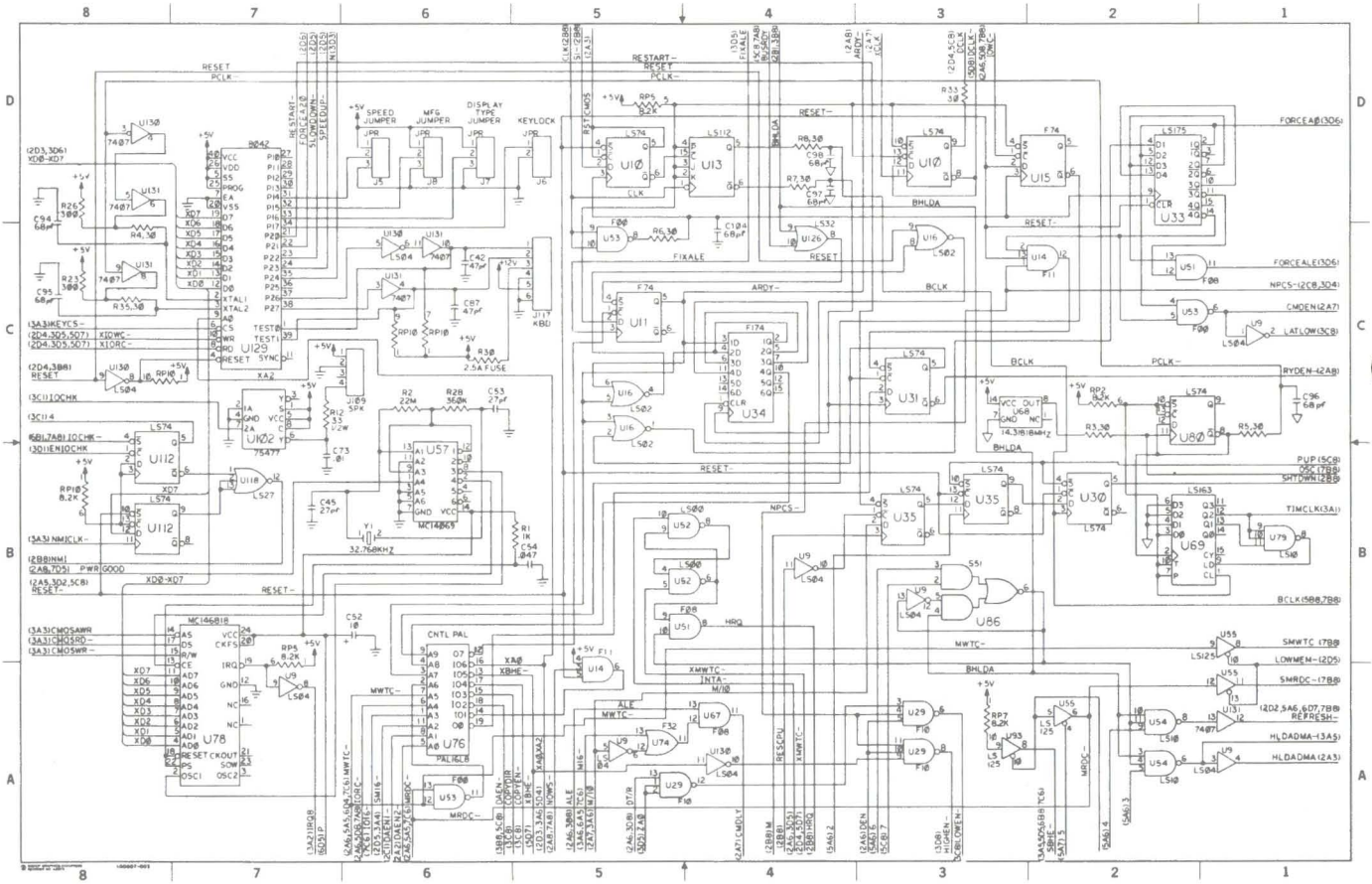


Figure 2-41. COMPAQ PORTABLE 286 System Board Schematics (Page 4 of 7)

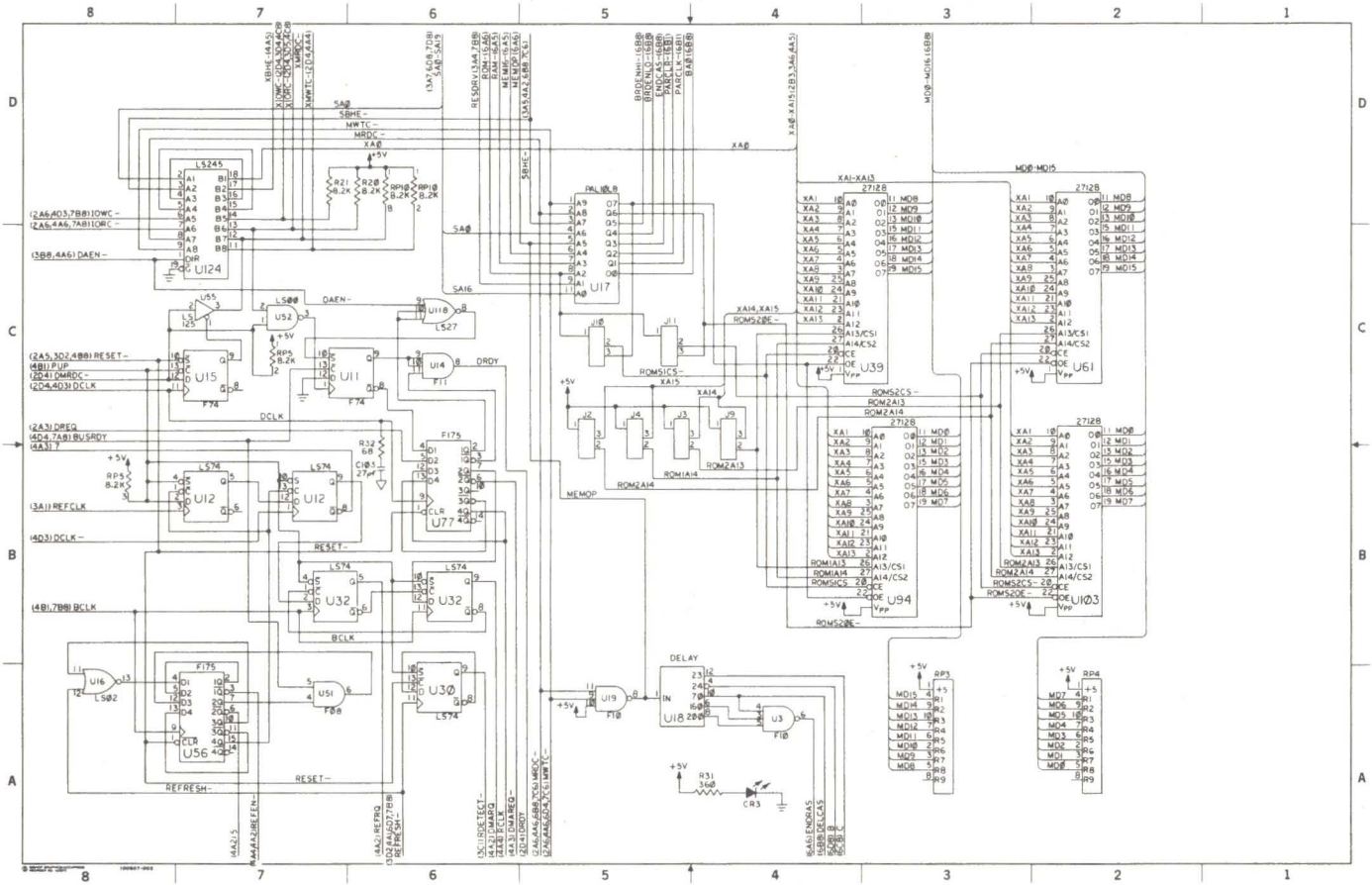


Figure 2-41. COMPAQ PORTABLE 286 System Board Schematics (Page 5 of 7)

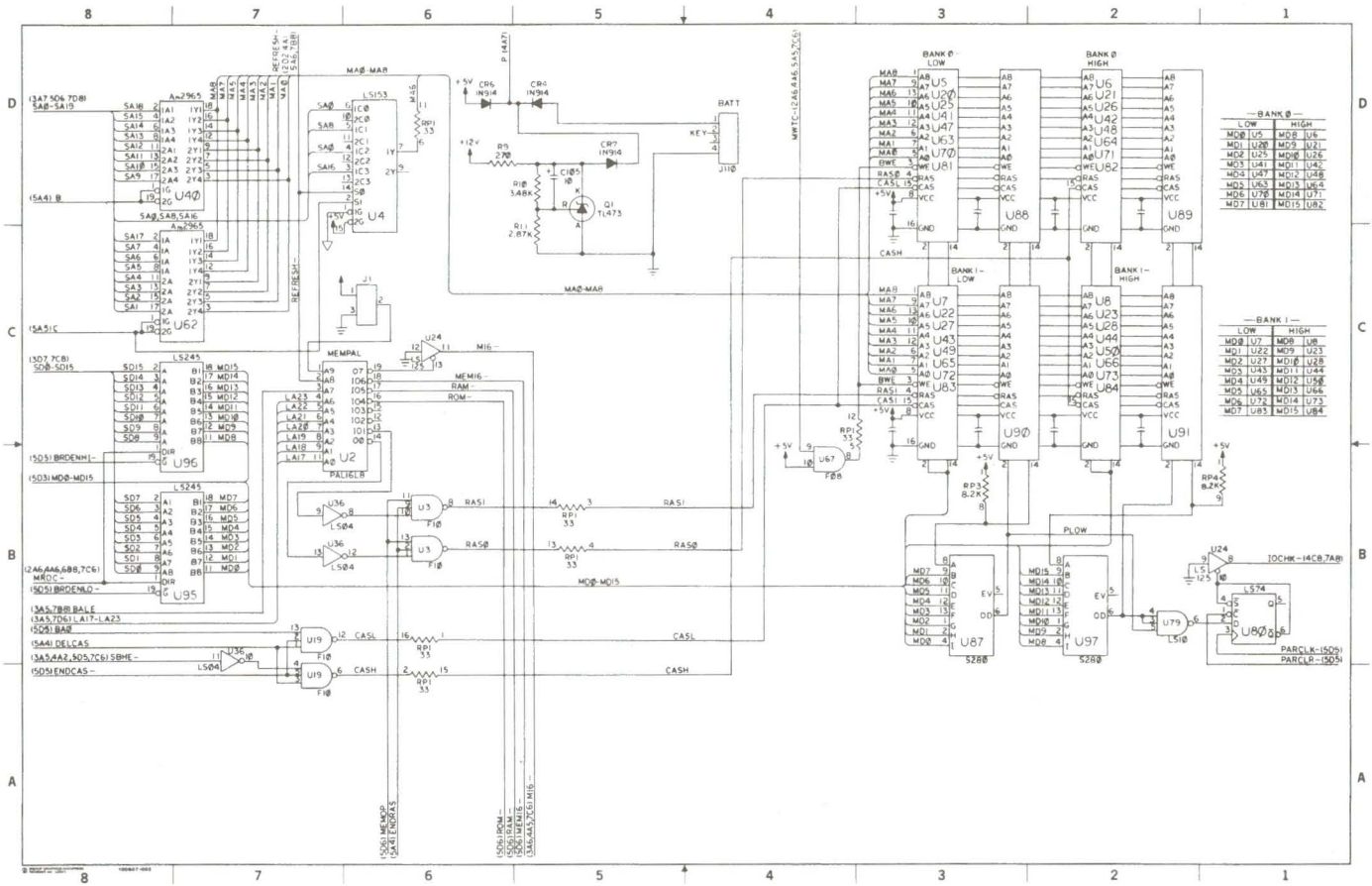


Figure 2-41. COMPAQ PORTABLE 286 System Board Schematics (Page 6 of 7)

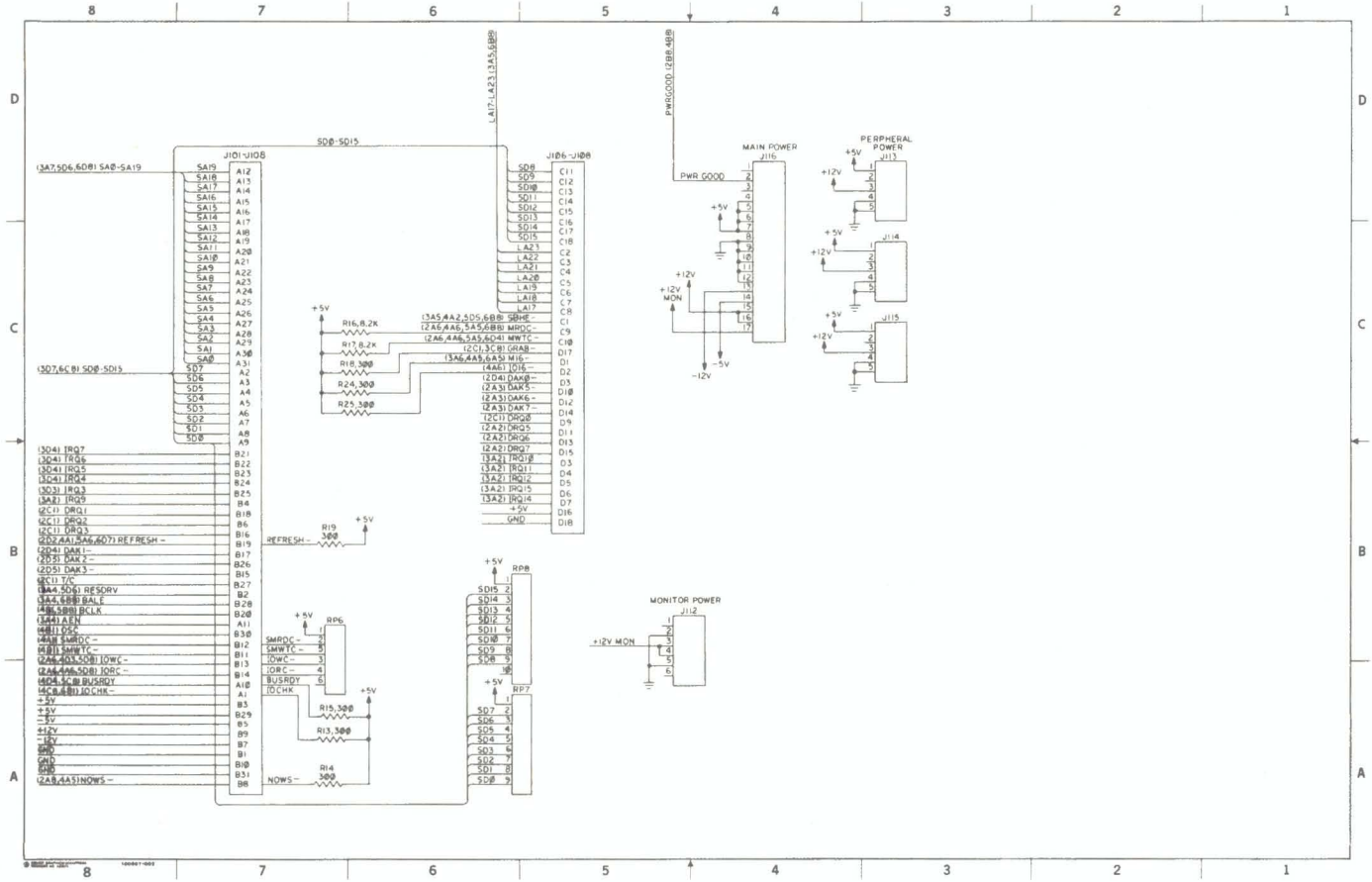


Figure 2-41. COMPAQ PORTABLE 286 System Board Schematics (Page 7 of 7)

Figure 2-42 shows the component layout for the COMPAQ DESKPRO 286 Version 1 System Board. Figure 2-43 shows the schematics for the COMPAQ DESKPRO 286 Version 1 System Board. Compaq Computer Corporation does not guarantee the accuracy of the component layout or the schematics. They are provided to aid in a general understanding of the system operation.

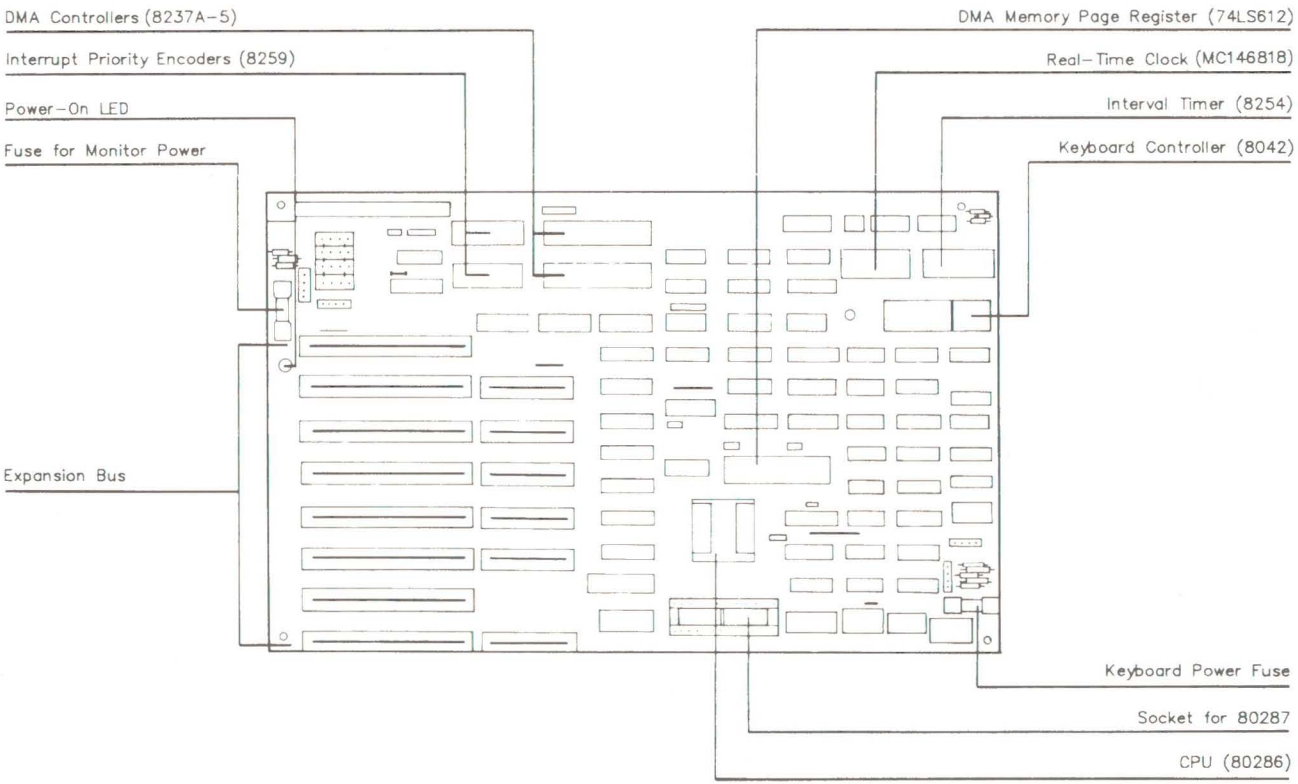


Figure 2-42. COMPAQ DESKPRO 286 Version 1 System Board Component Layout (Page 1 of 1)

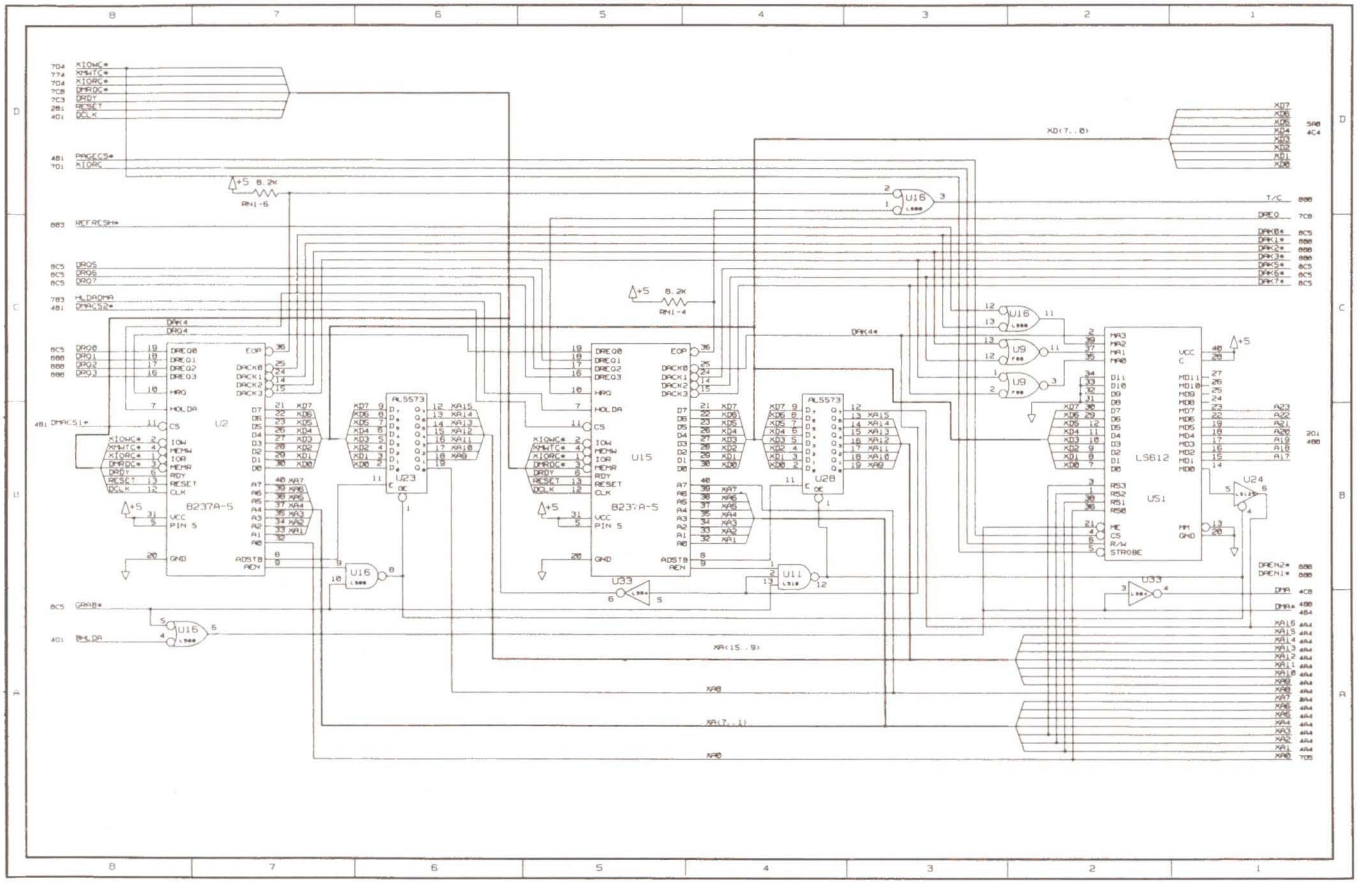


Figure 2-43. COMPAQ DESKPRO 286 Version 1 System Board Schematics (Page 3 of 8)

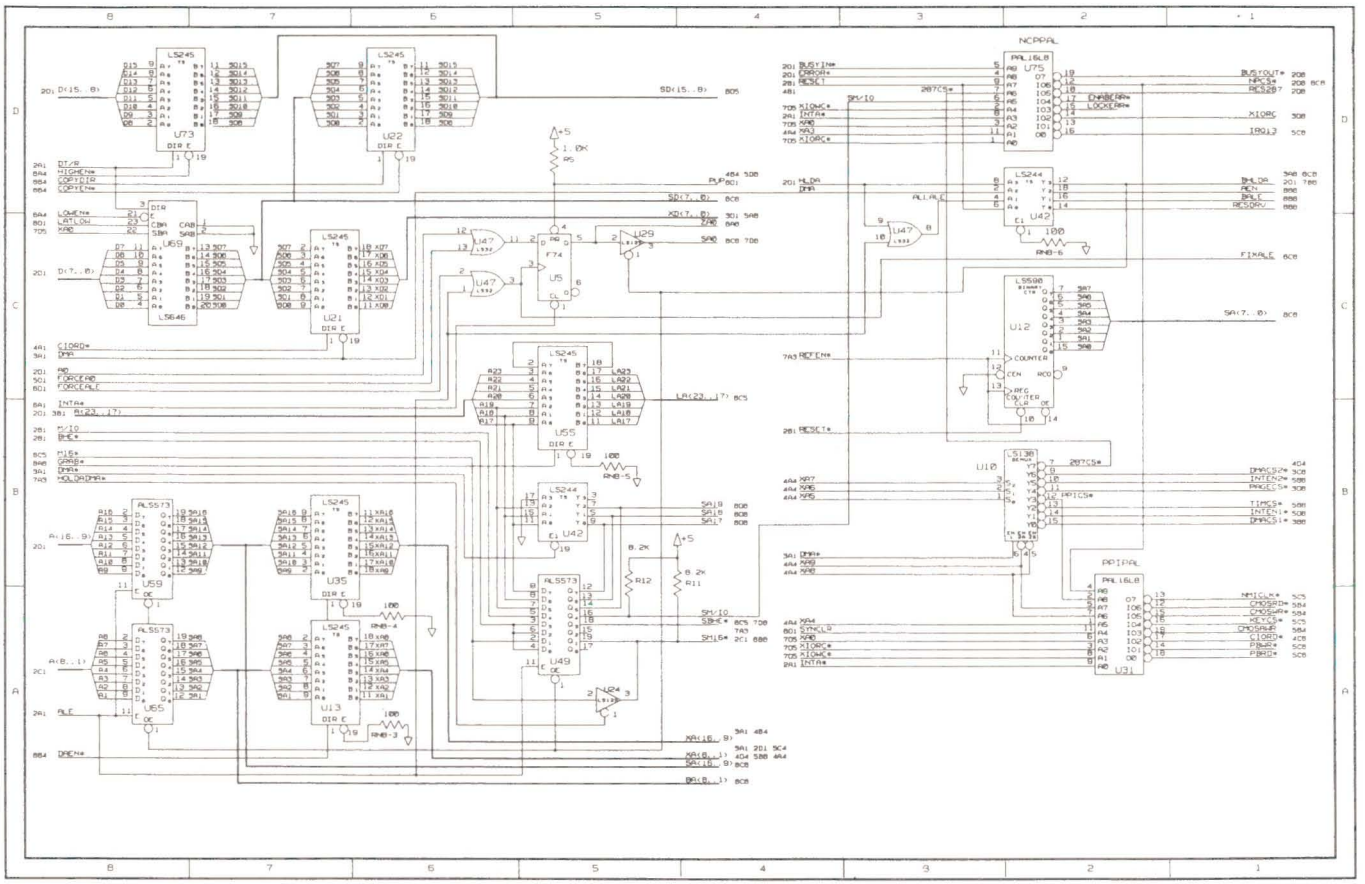


Figure 2-43. COMPAQ DESKPRO 286 Version 1 System Board Schematics (Page 4 of 8)

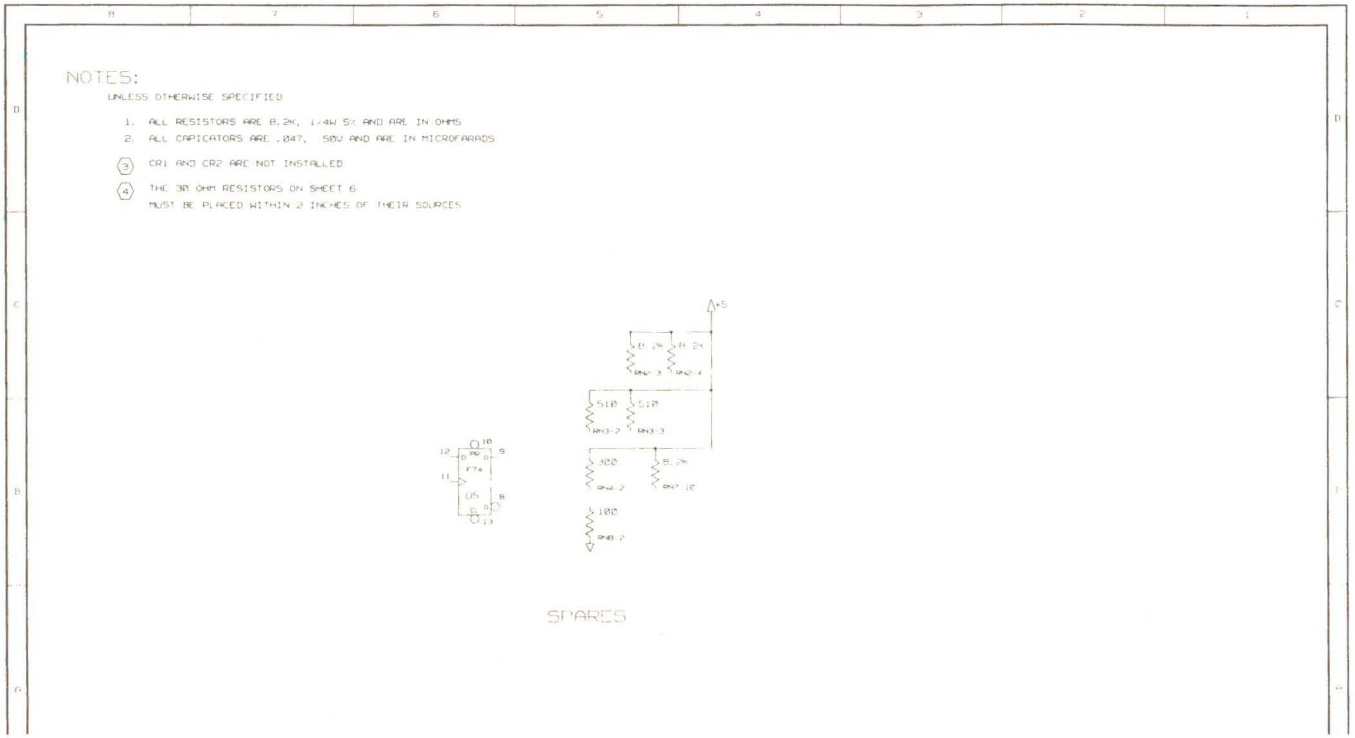


Figure 2-43. COMPAQ DESKPRO 286 Version 1 System Board Schematics (Page 1 of 8)

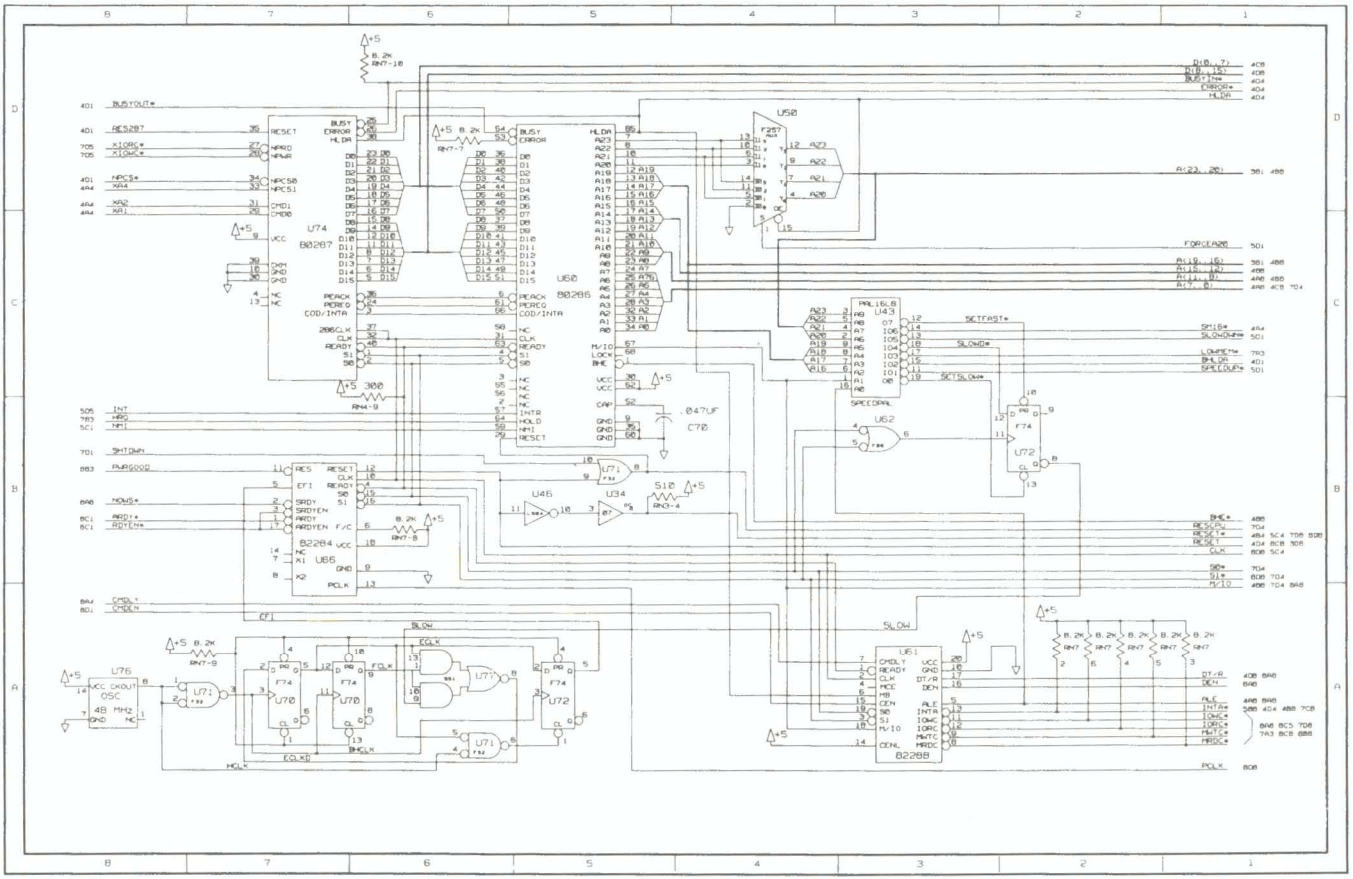


Figure 2-43. COMPAQ DESKPRO 286 Version 1 System Board Schematics (Page 2 of 8)

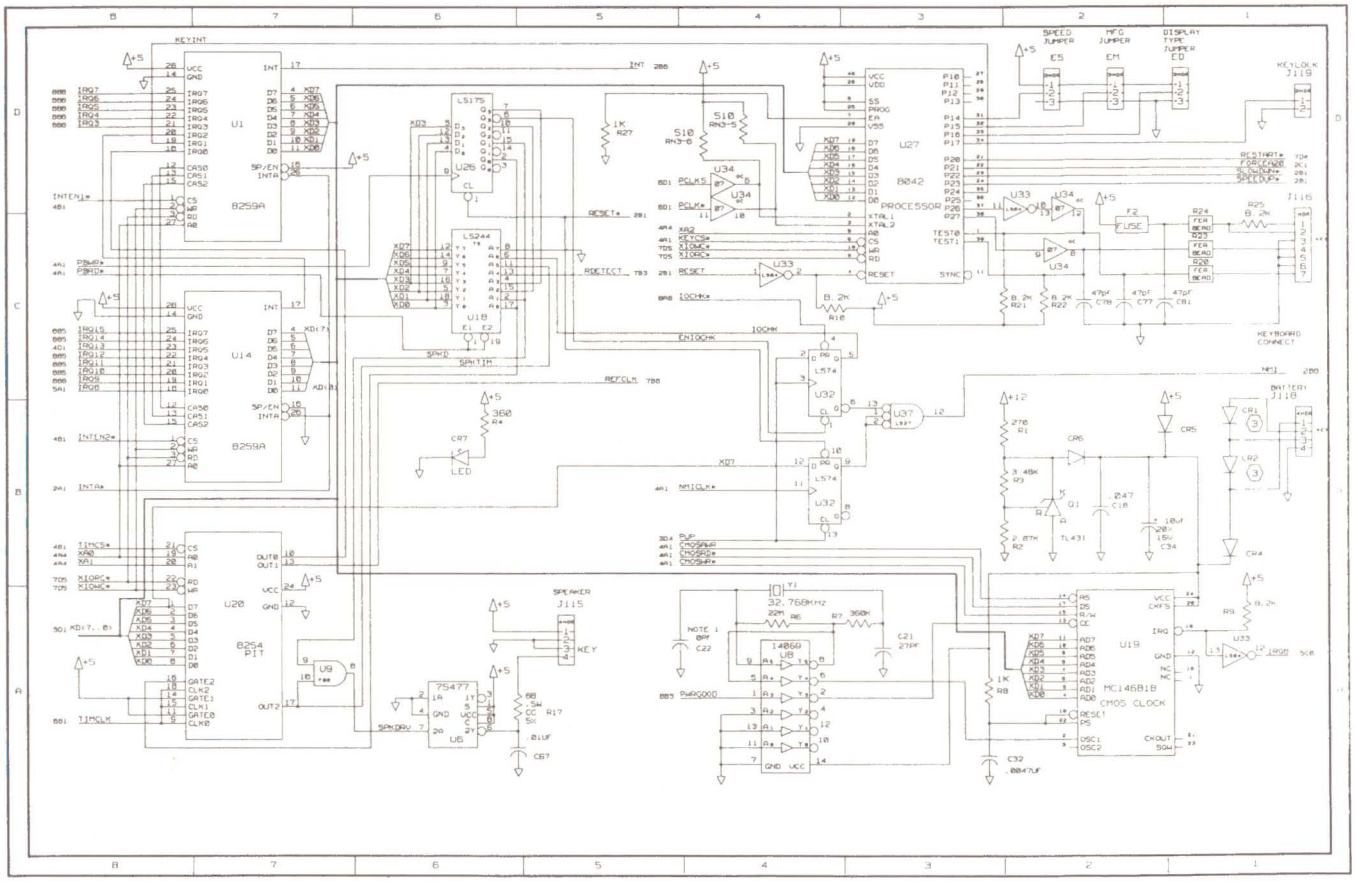


Figure 2-43. COMPAQ DESKPRO 286 Version 1 System Board Schematics (Page 5 of 8)

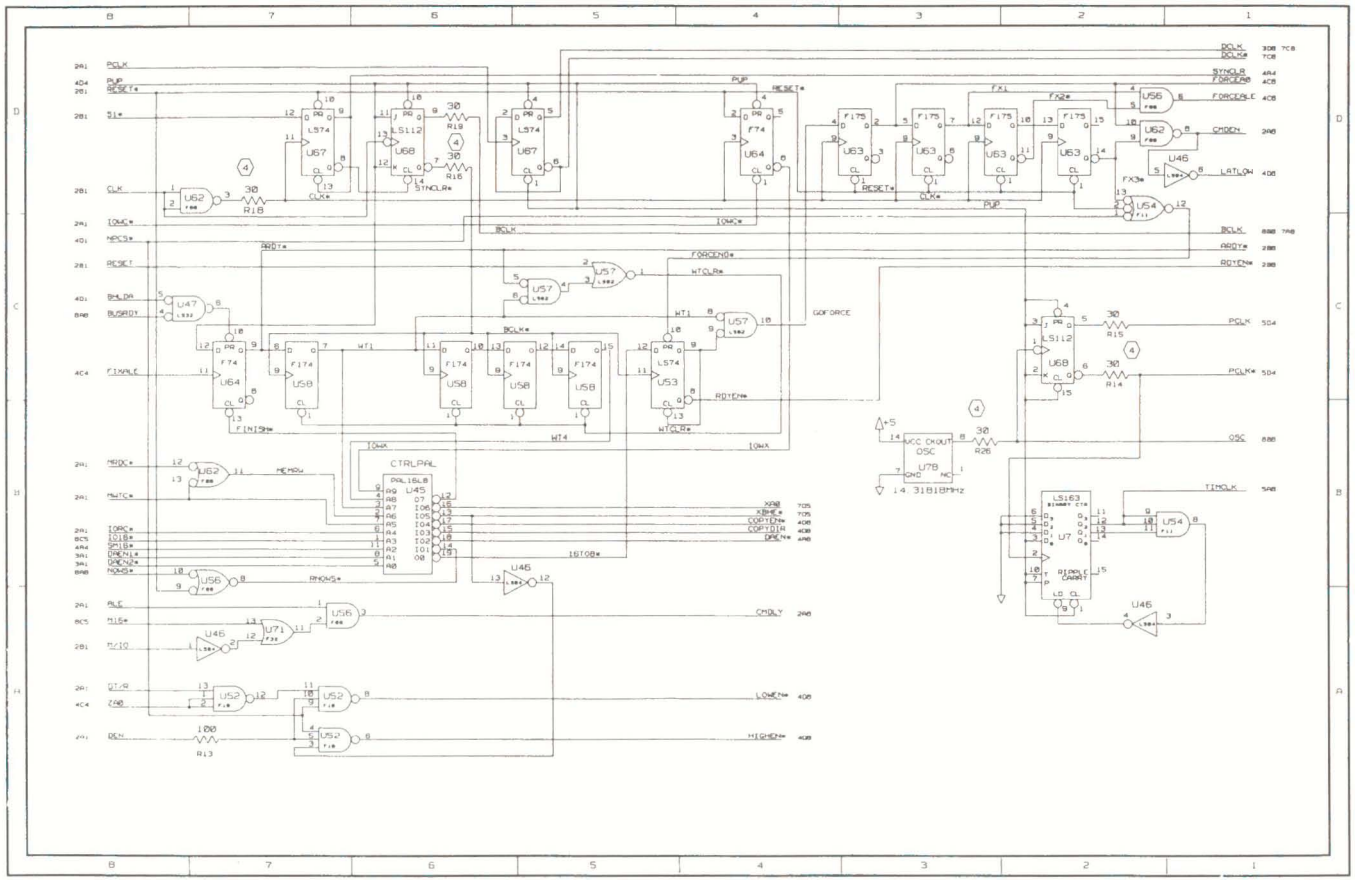


Figure 2-43. COMPAQ DESKPRO 286 Version 1 System Board Schematics (Page 6 of 8)

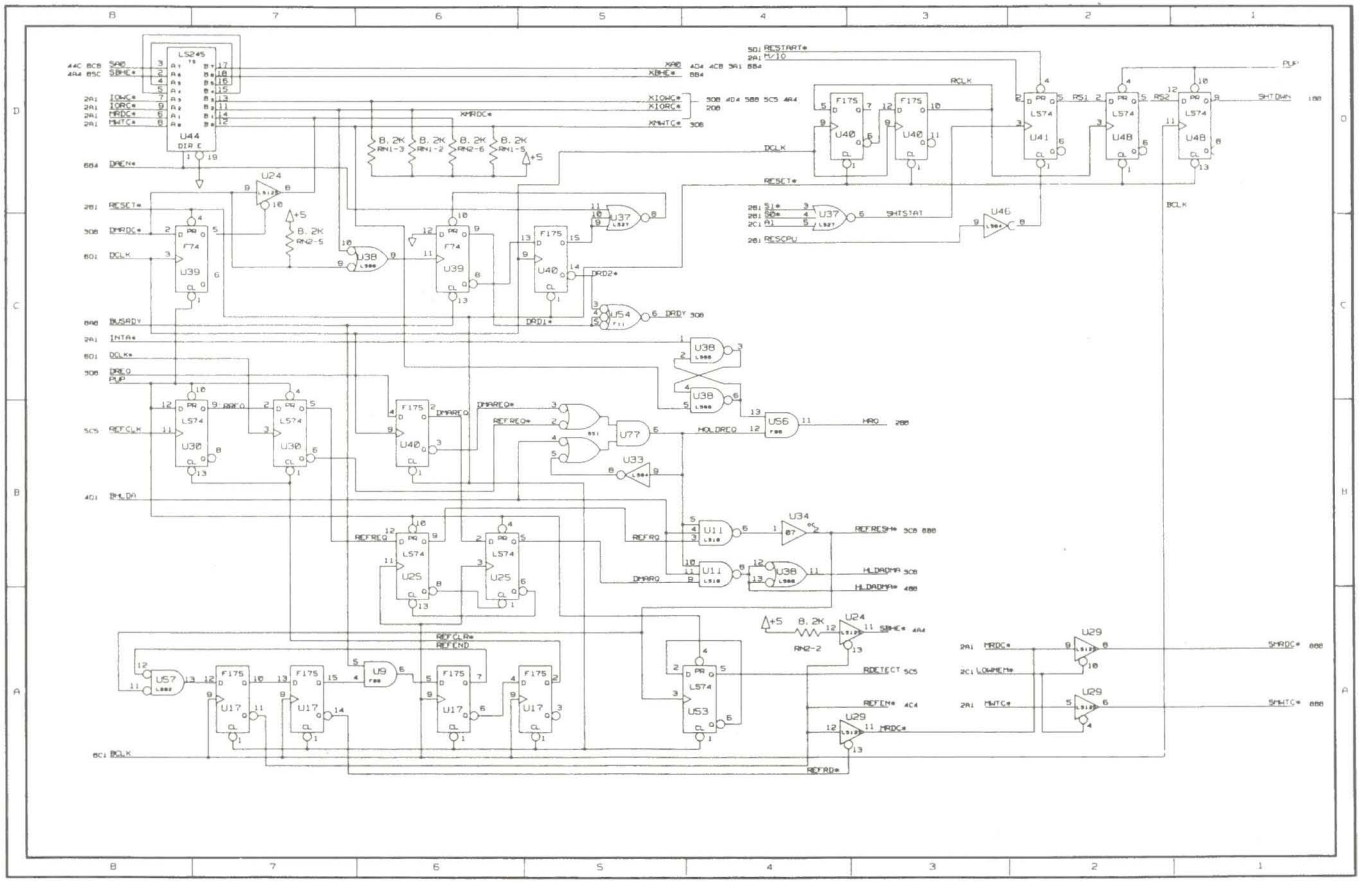


Figure 2-43. COMPAQ DESKPRO 286 Version 1 System Board Schematics (Page 7 of 8)

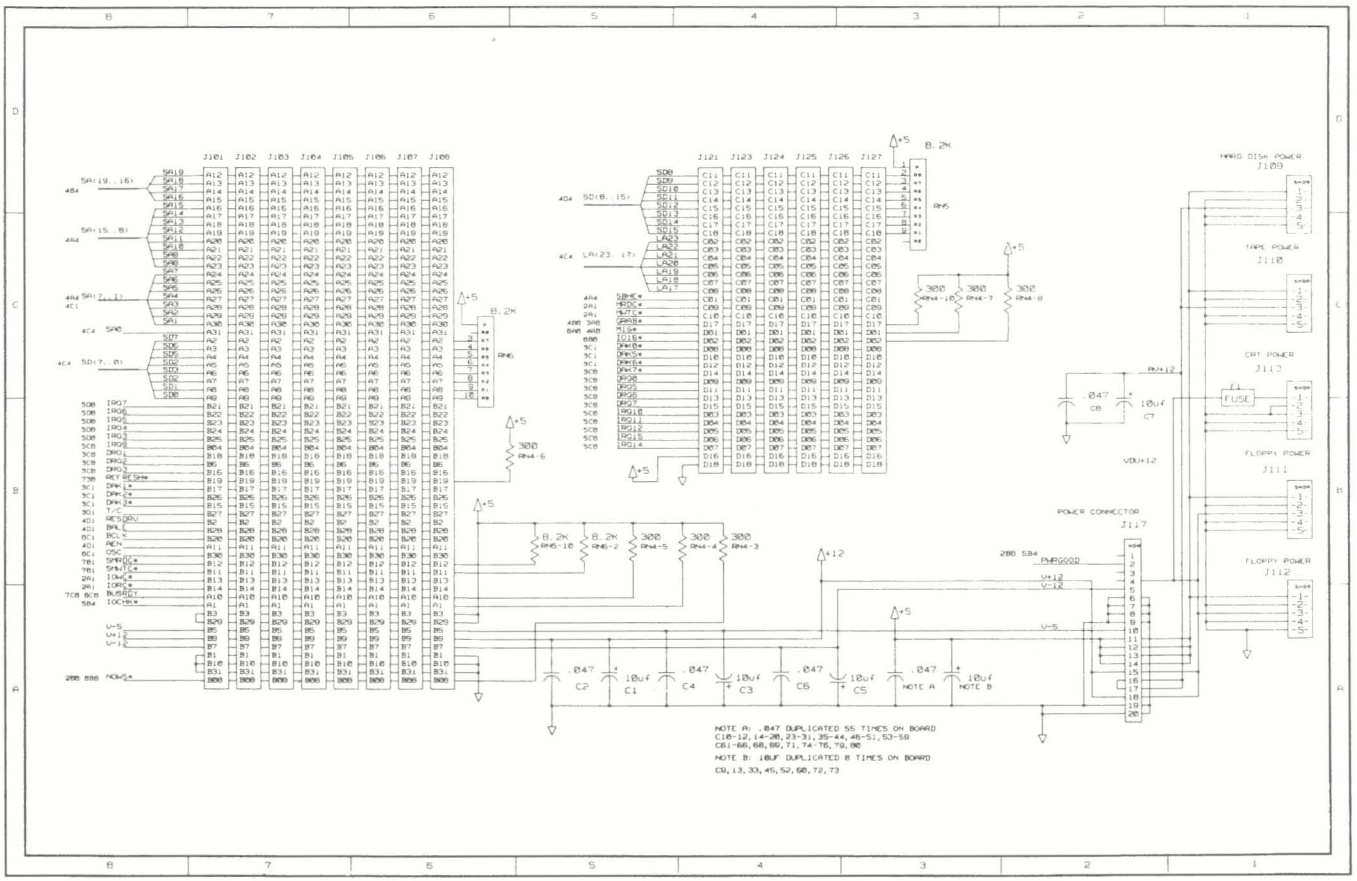


Figure 2-43. COMPAQ DESKPRO 286 Version 1 System Board Schematics (Page 8 of 8)

Figure 2-44 shows the component layout for the COMPAQ DESKPRO 286 Version 2 System Board. Figure 2-45 shows the schematics for the COMPAQ DESKPRO 286 Version 2 System Board. Compaq Computer Corporation does not guarantee the accuracy of the component layout or the schematics. They are provided to aid in a general understanding of the system operation.

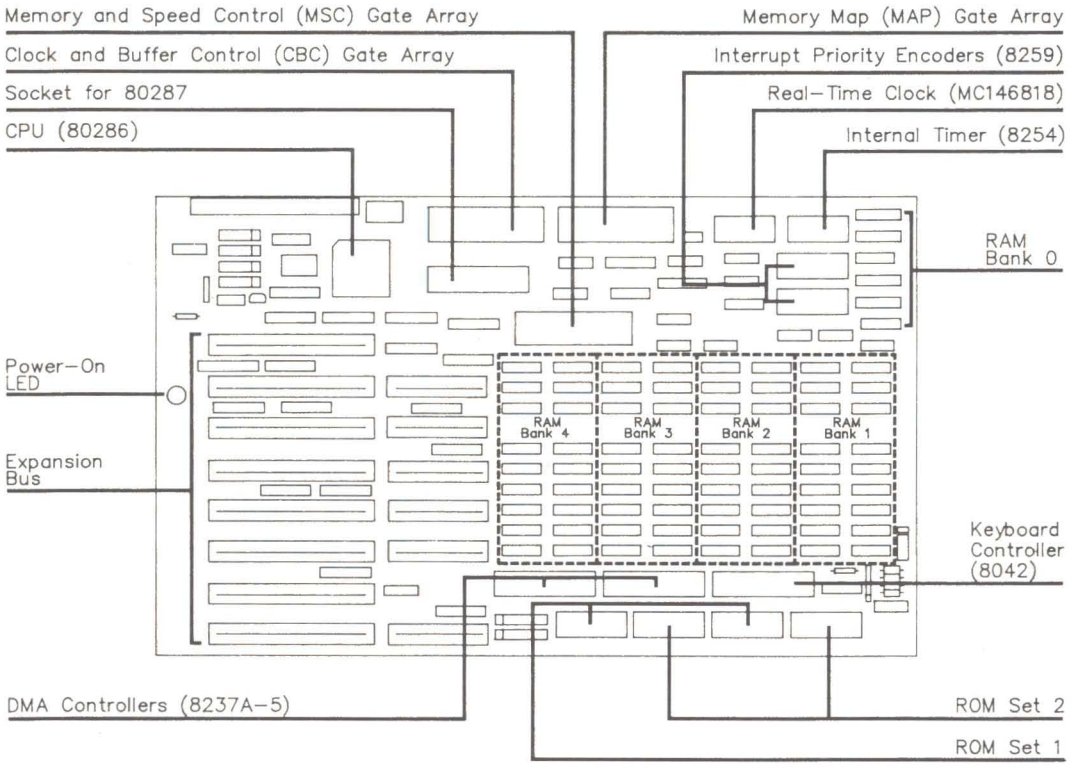


Figure 2-44. COMPAQ DESKPRO 286 Version 2 System Board Component Layout (Page 1 of 1)

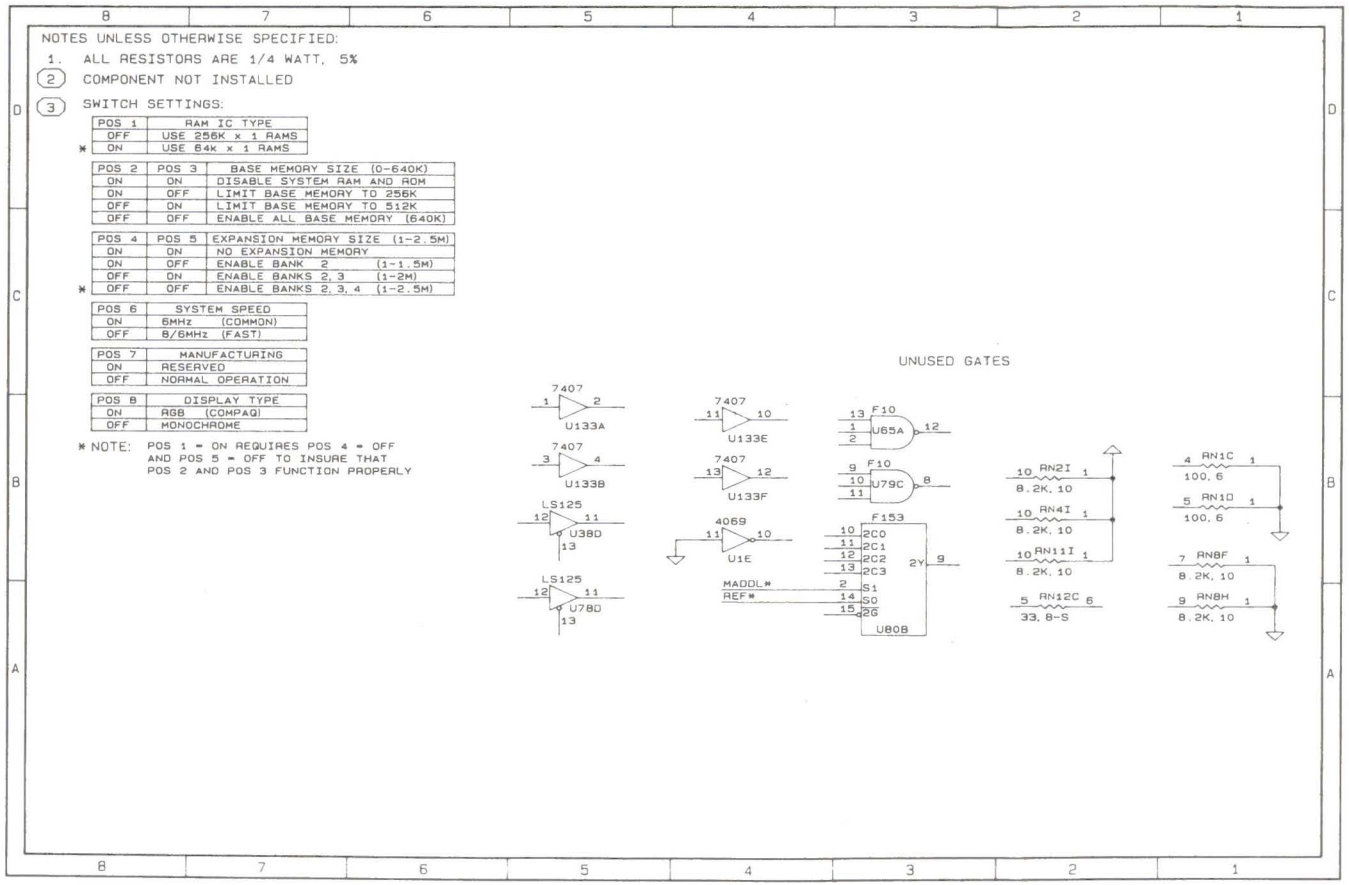


Figure 2-45. COMPAQ DESKPRO 286 Version 2 System Board Schematics (Page 1 of 18)

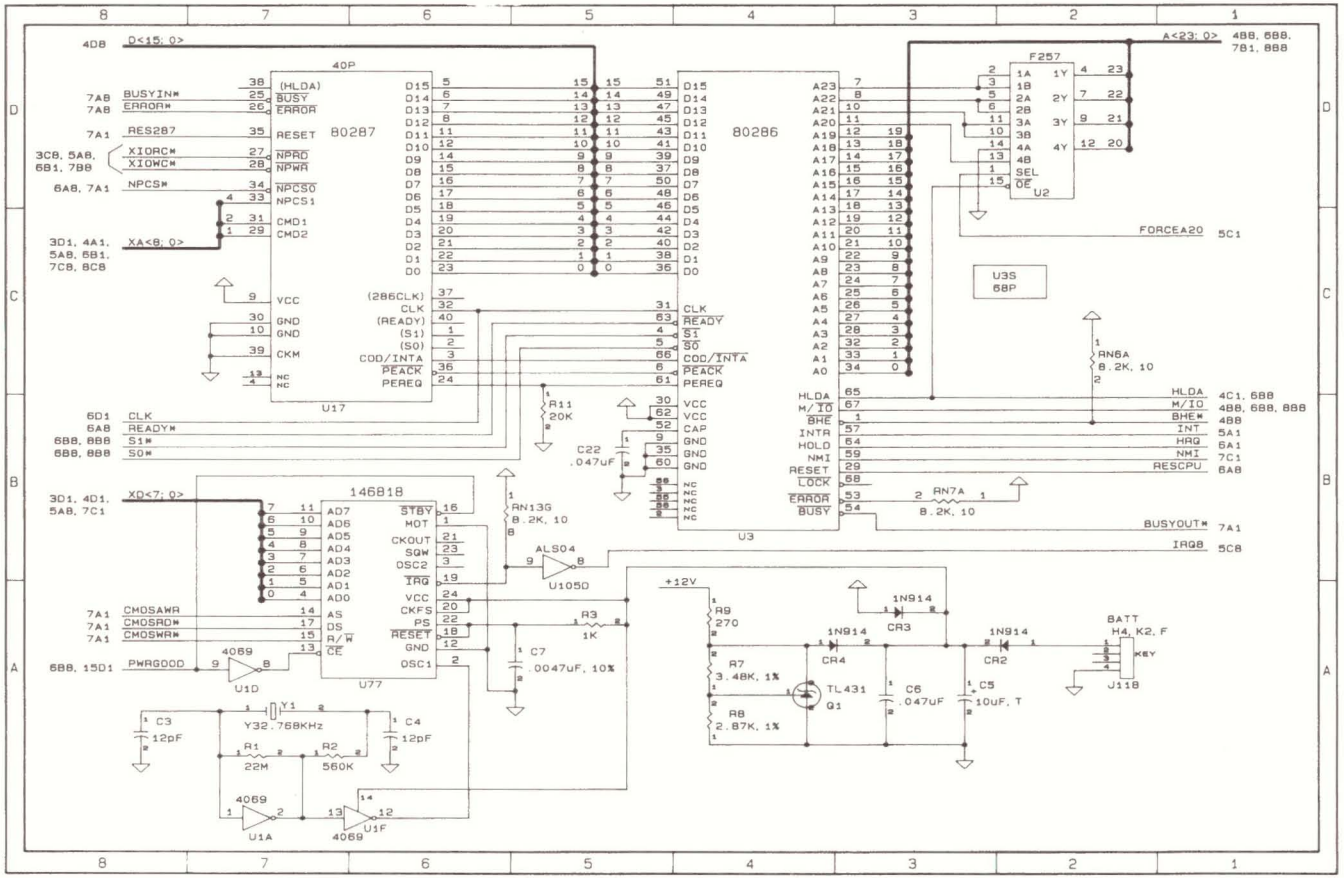


Figure 2-45. COMPAQ DESKPRO 286 Version 2 System Board Schematics (Page 2 of 18)

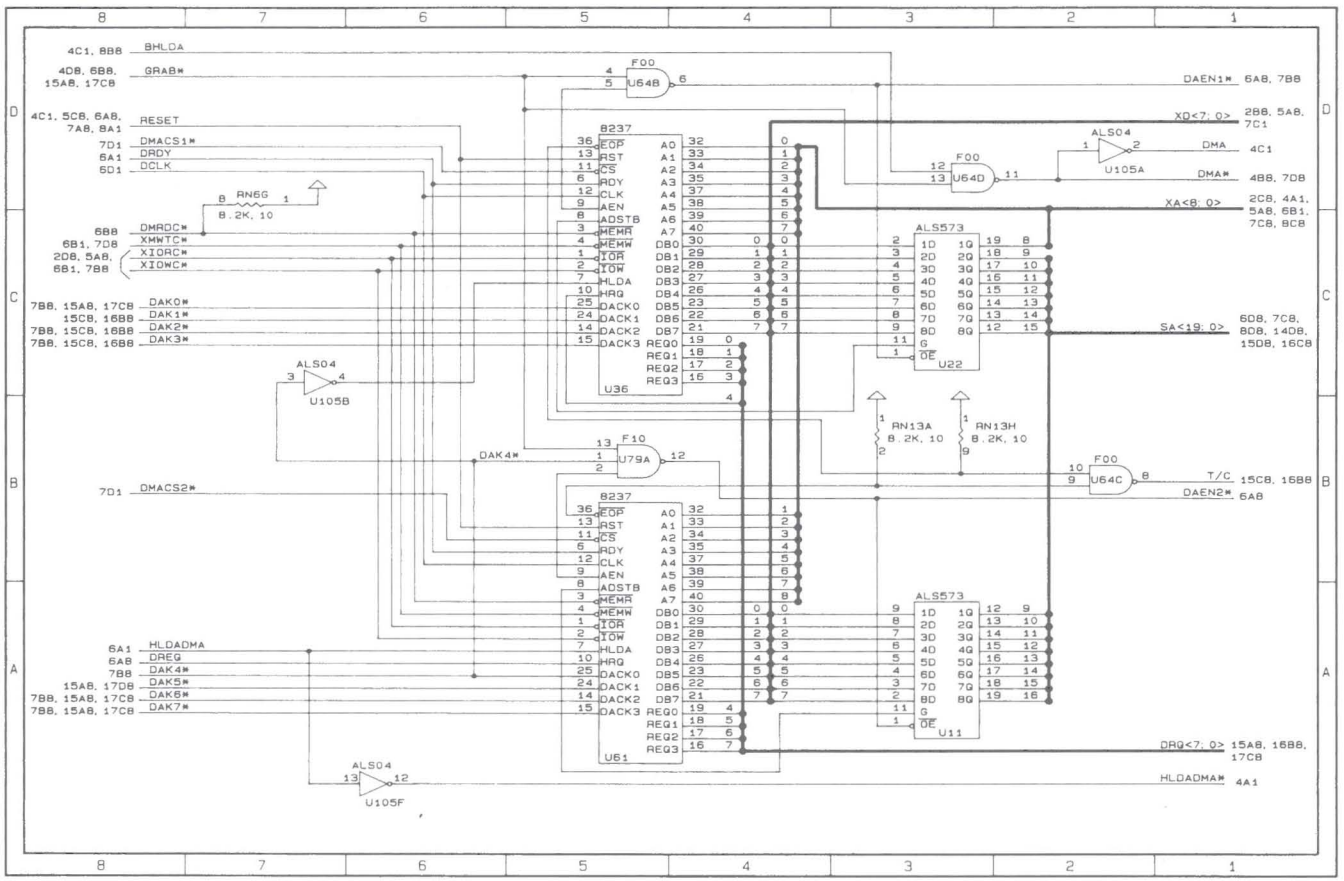


Figure 2-45. COMPAQ DESKPRO 286 Version 2 System Board Schematics (Page 3 of 18)

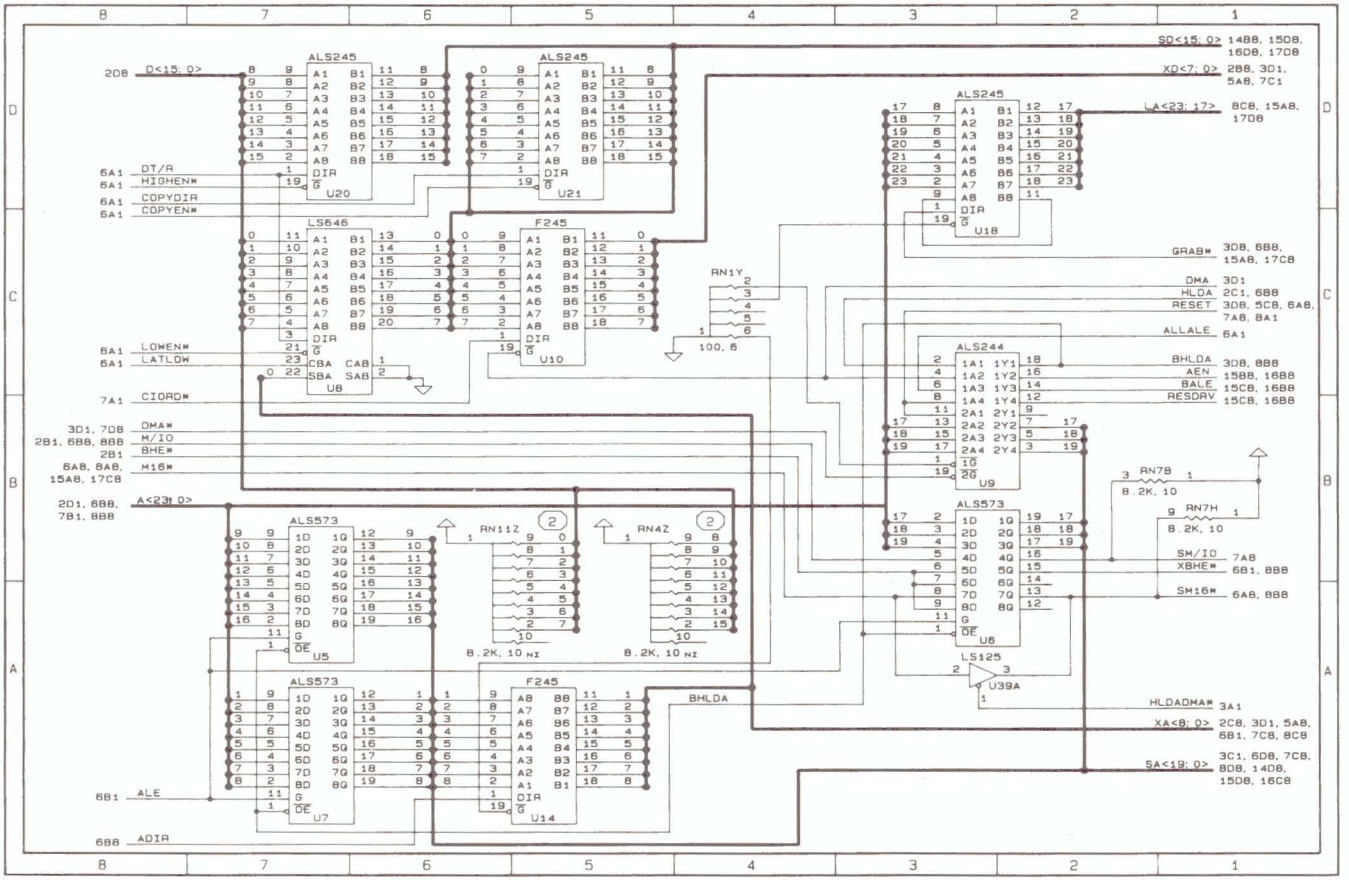


Figure 2-45. COMPAQ DESKPRO 286 Version 2 System Board Schematics (Page 4 of 18)

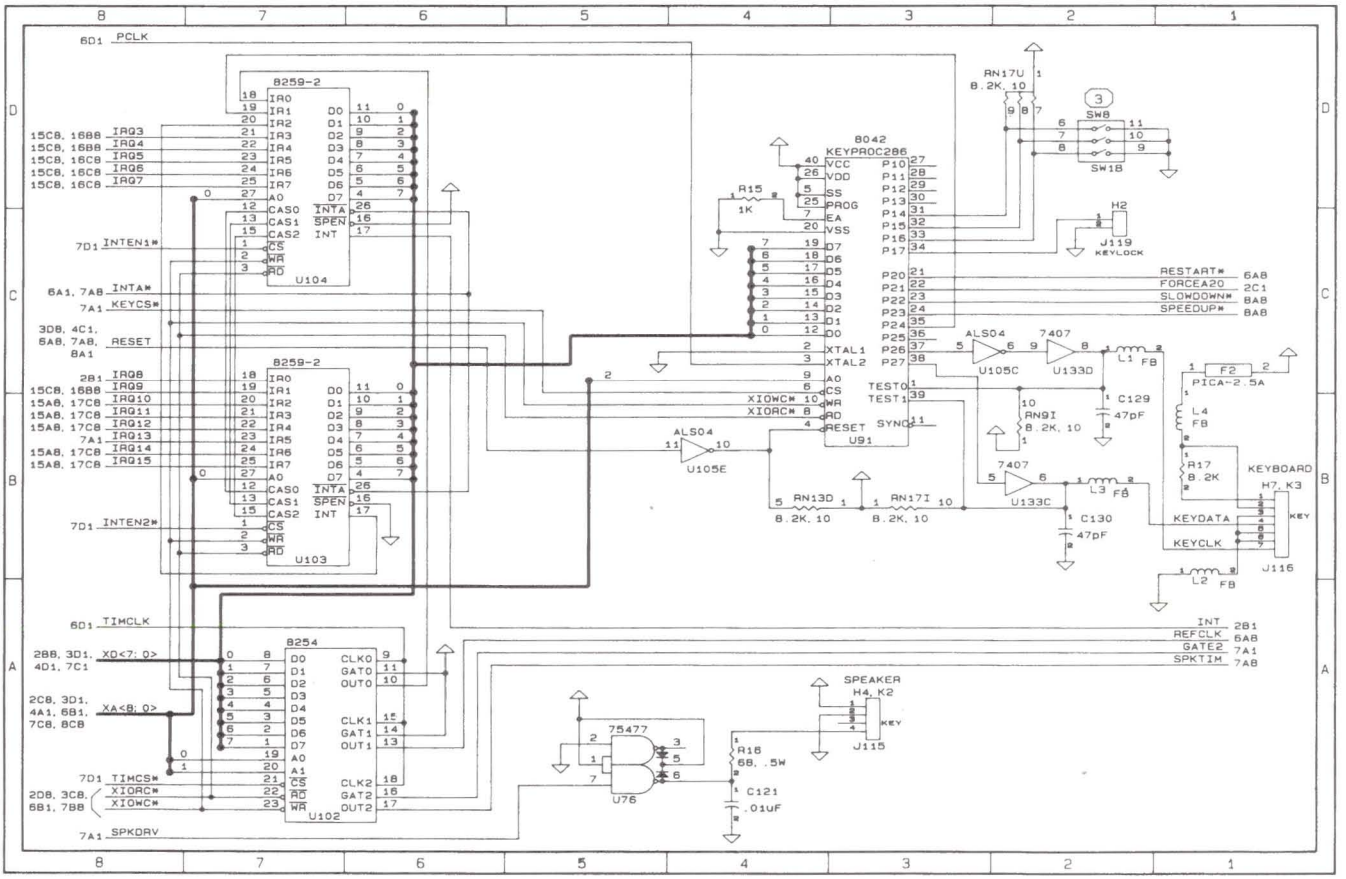


Figure 2-45. COMPAQ DESKPRO 286 Version 2 System Board Schematics (Page 5 of 18)

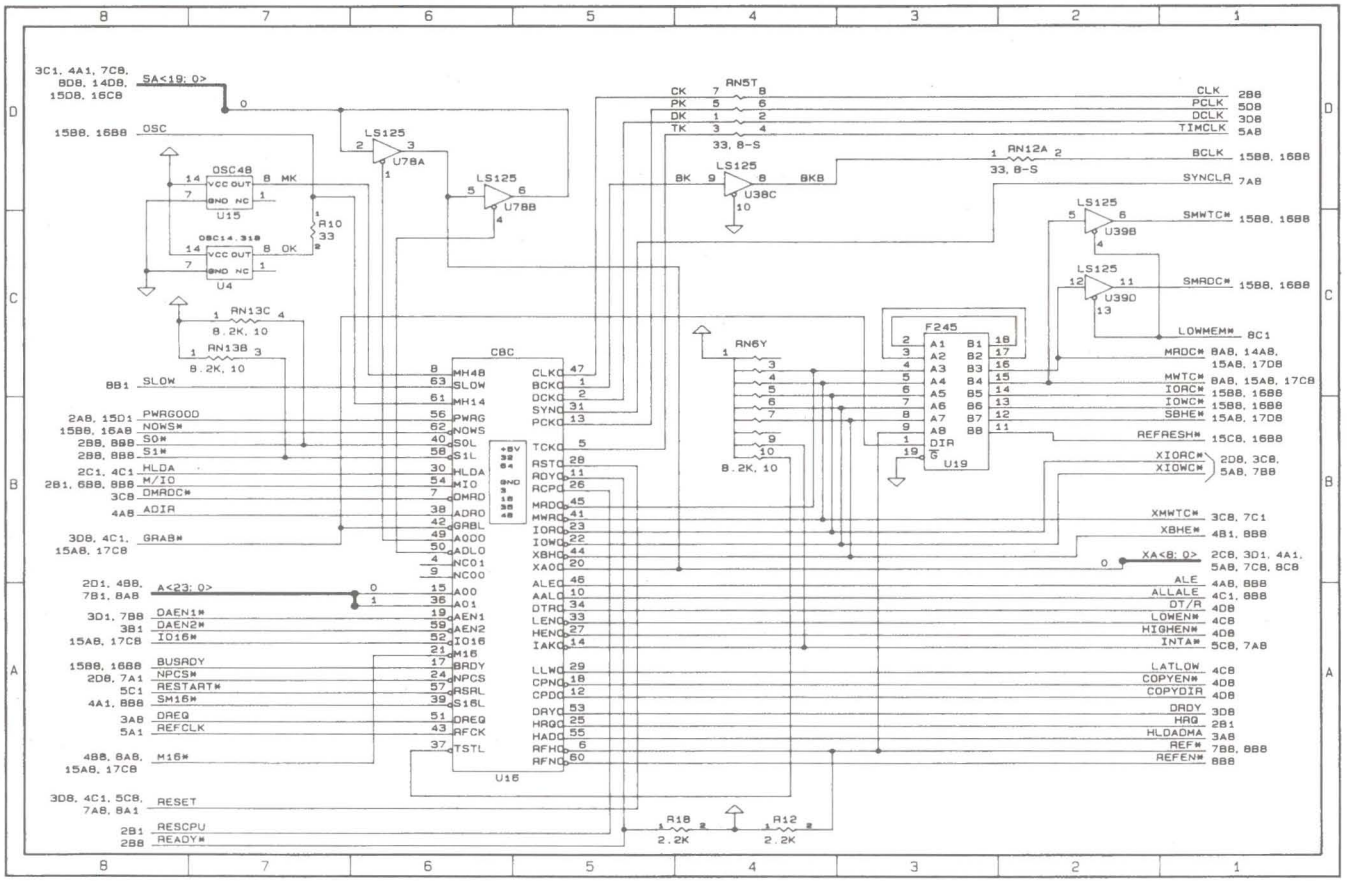


Figure 2-45. COMPAQ DESKPRO 286 Version 2 System Board Schematics (Page 6 of 18)

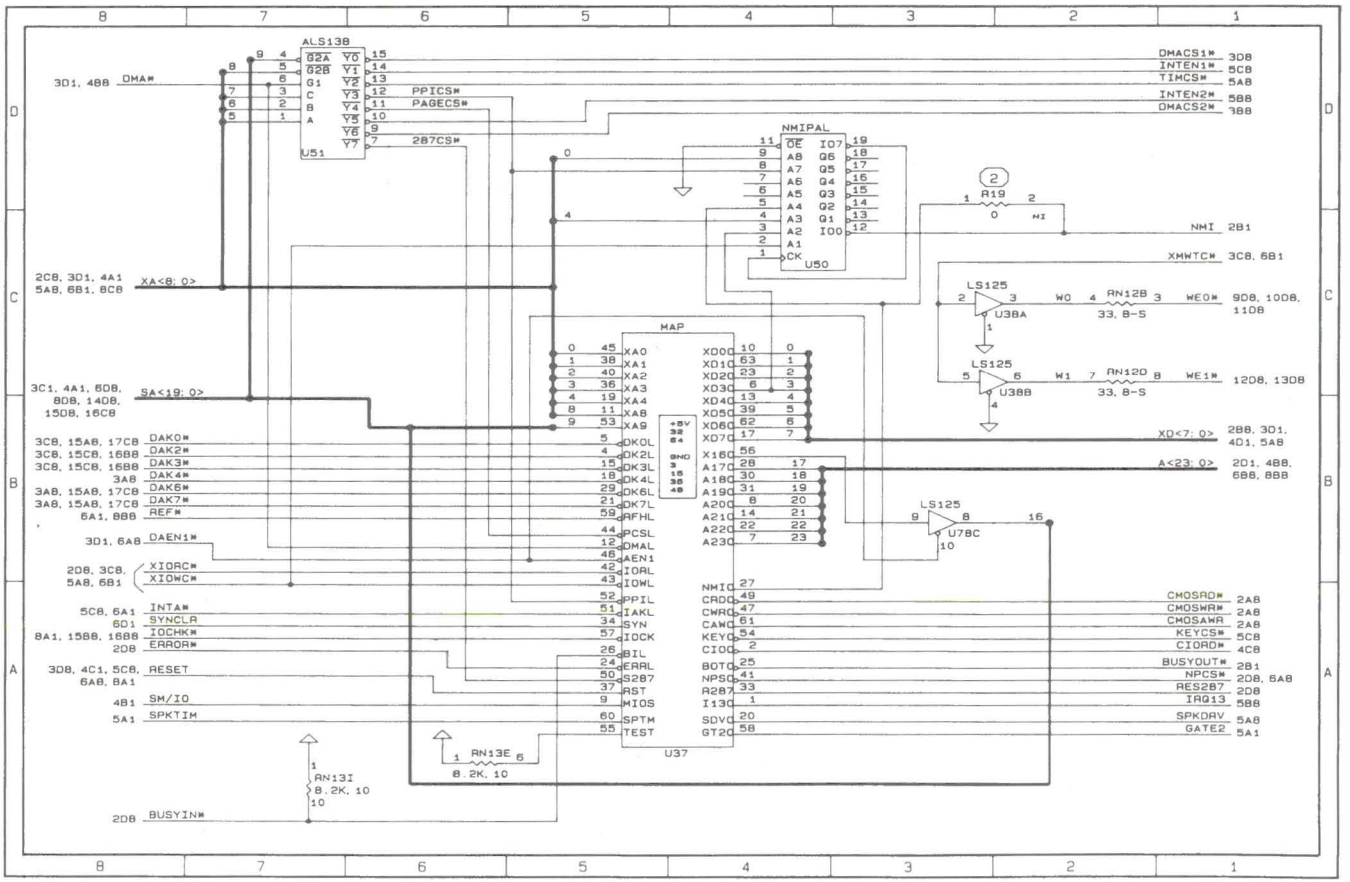


Figure 2-45. COMPAQ DESKPRO 286 Version 2 System Board Schematics (Page 7 of 18)

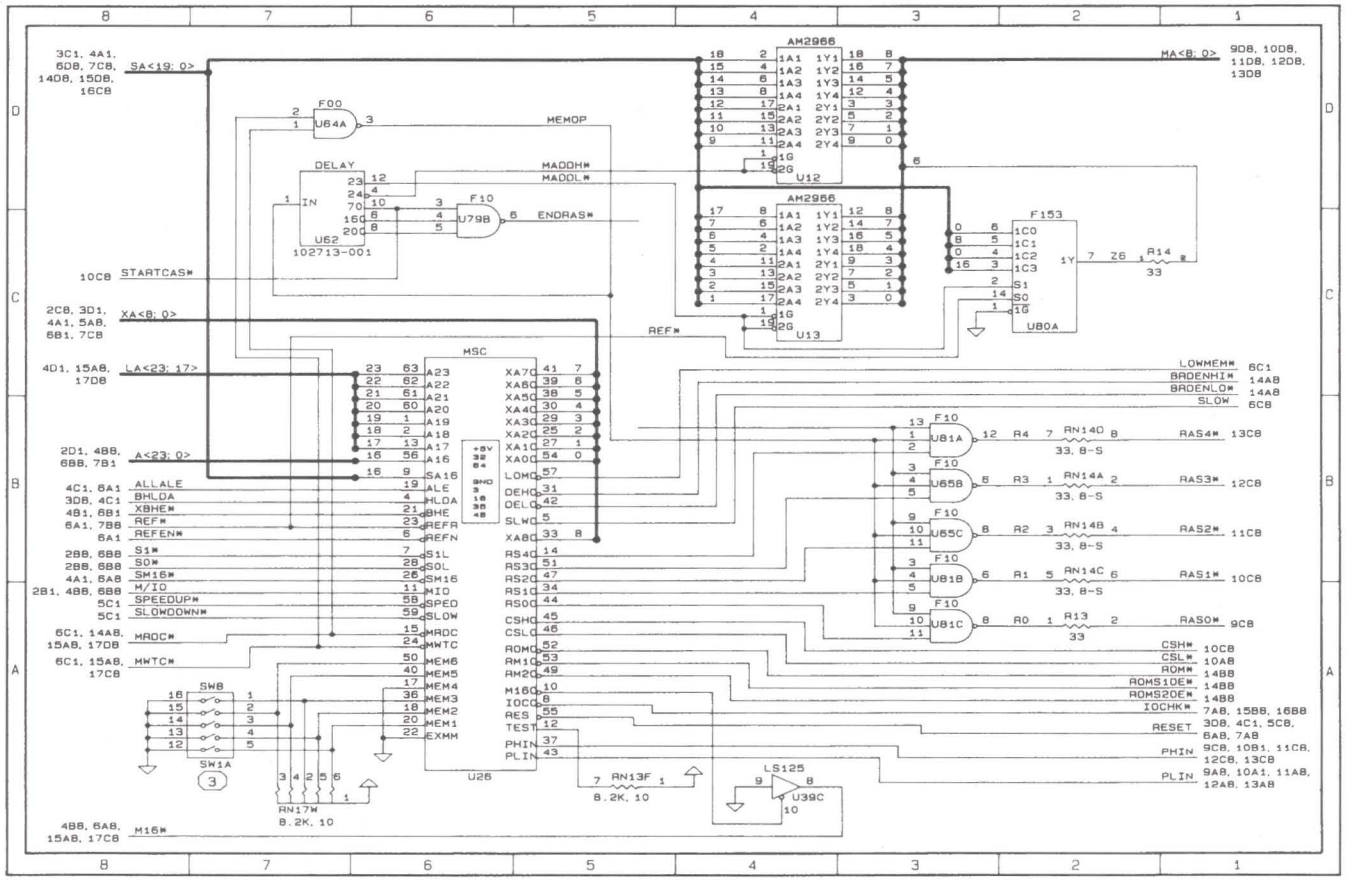


Figure 2-45. COMPAQ DESKPRO 286 Version 2 System Board Schematics (Page 8 of 18)

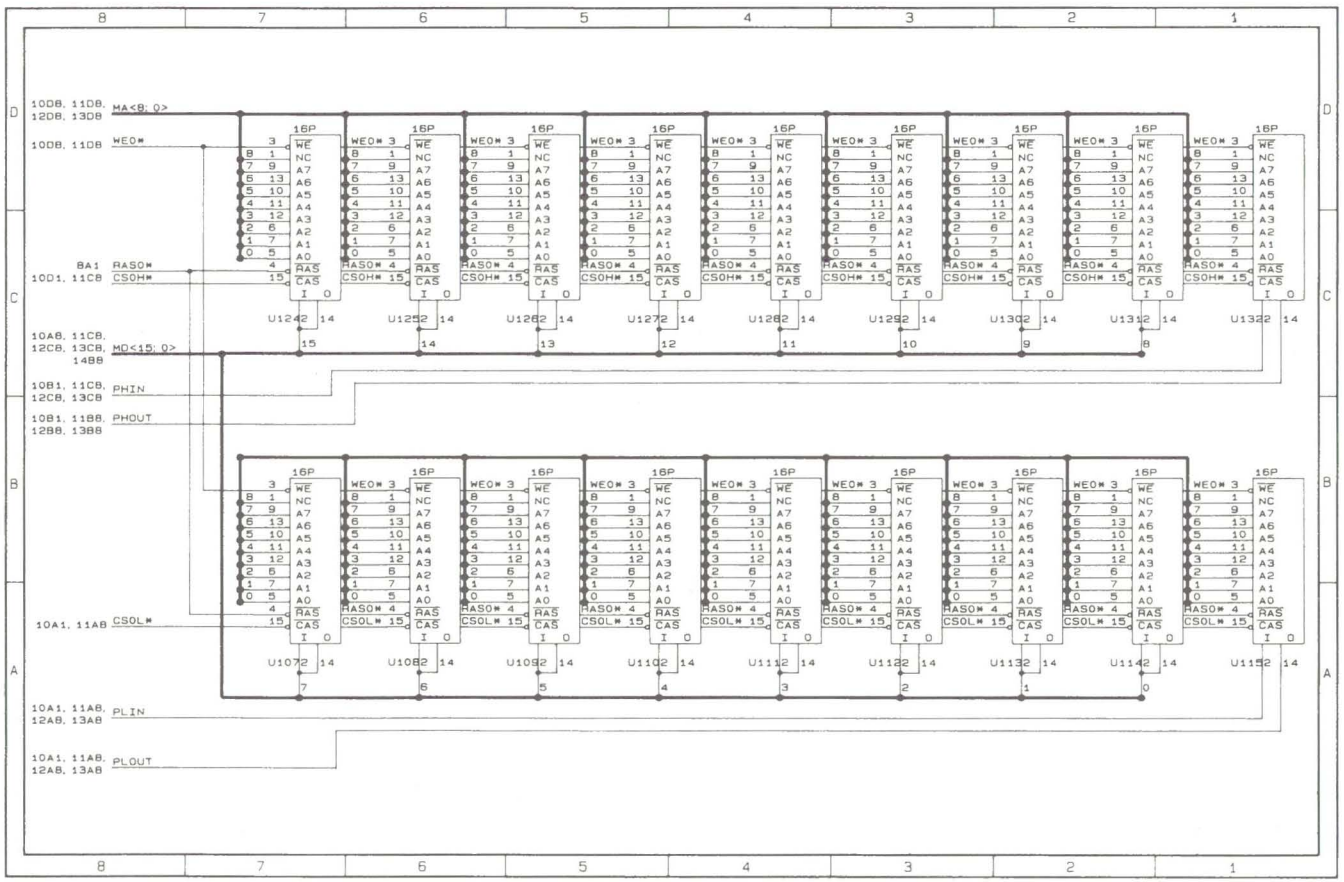


Figure 2-45. COMPAQ DESKPRO 286 Version 2 System Board Schematics (Page 9 of 18)

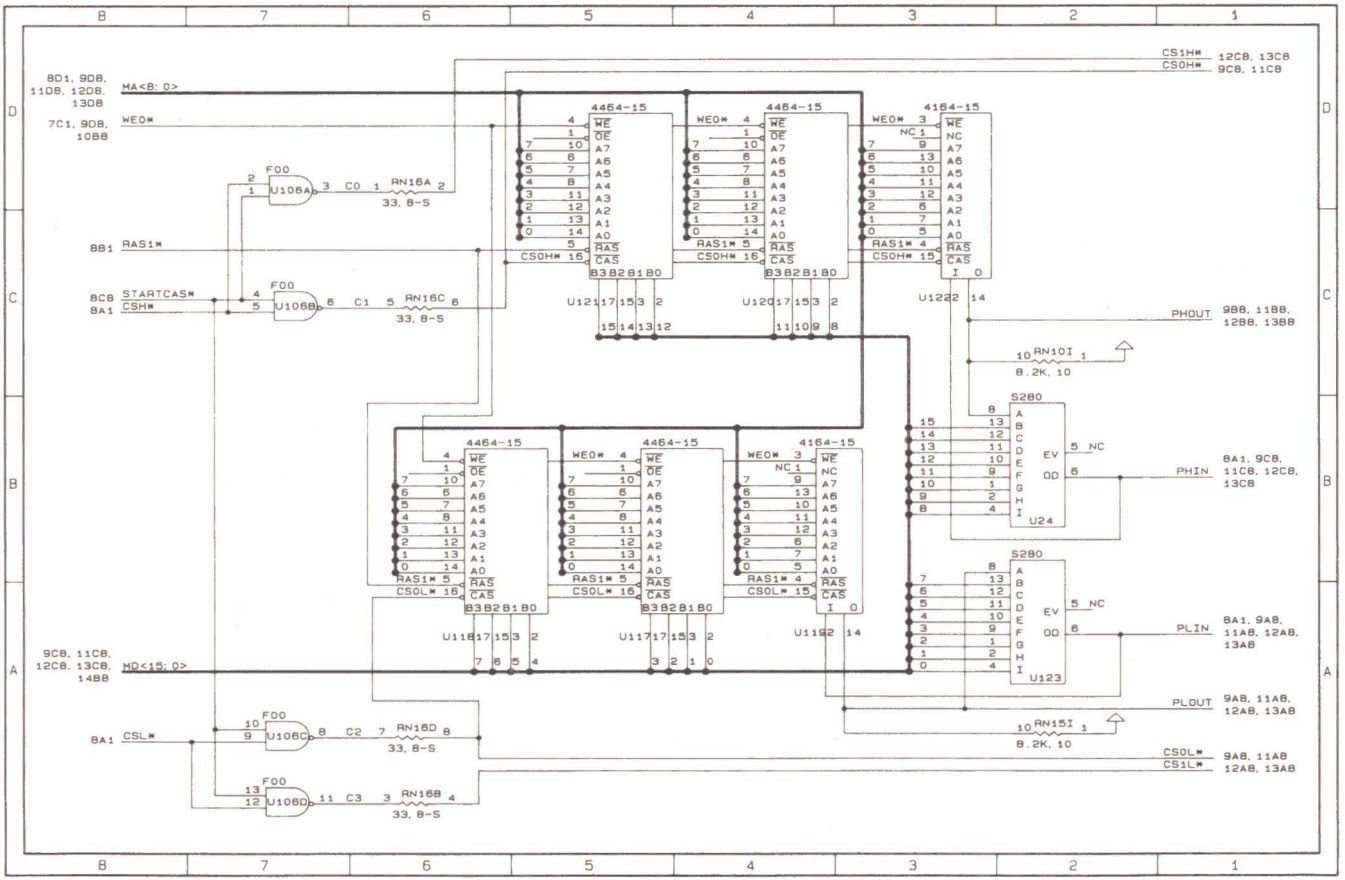


Figure 2-45. COMPAQ DESKPRO 286 Version 2 System Board Schematics (Page 10 of 18)

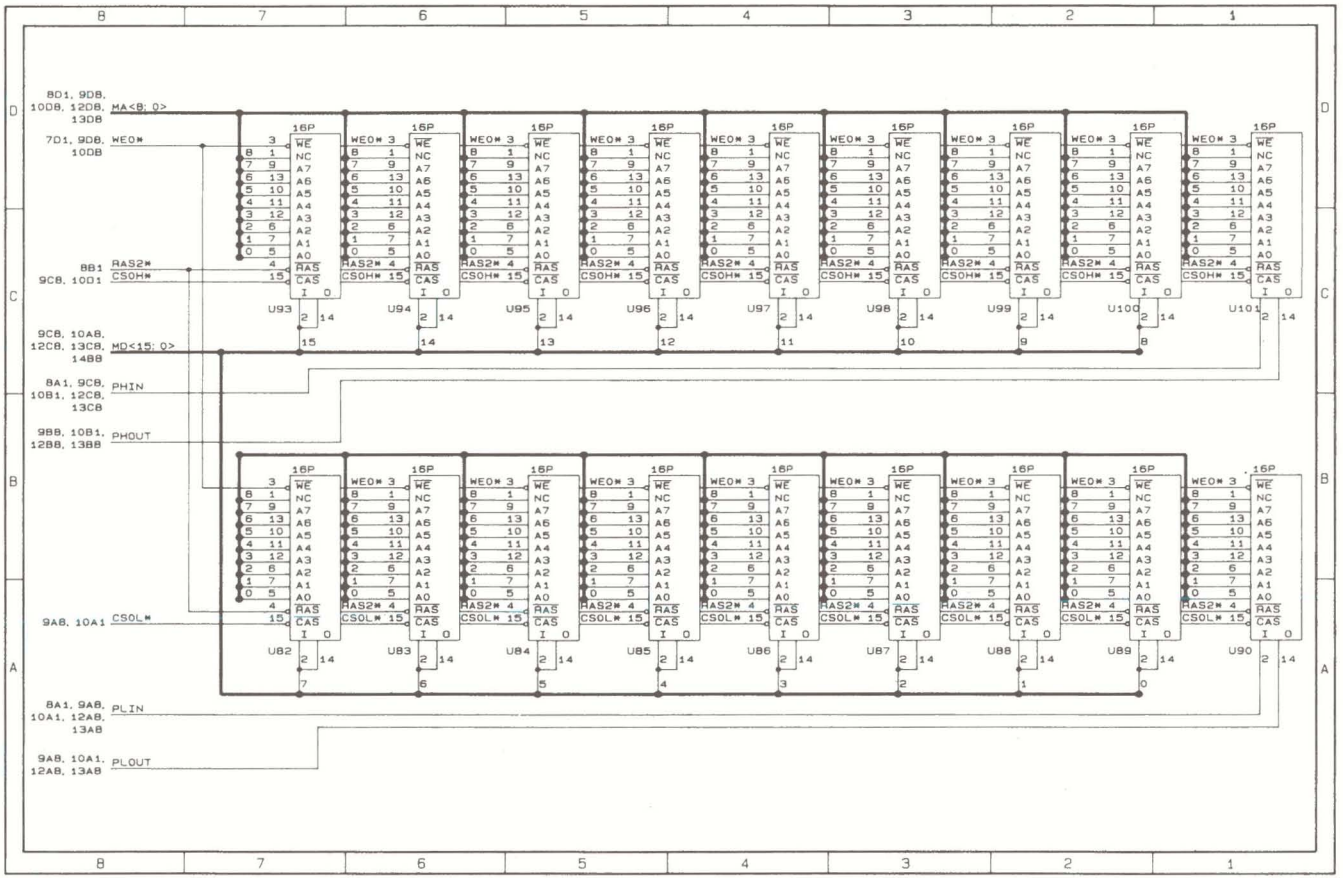


Figure 2-45. COMPAQ DESKPRO 286 Version 2 System Board Schematics (Page 11 of 18)

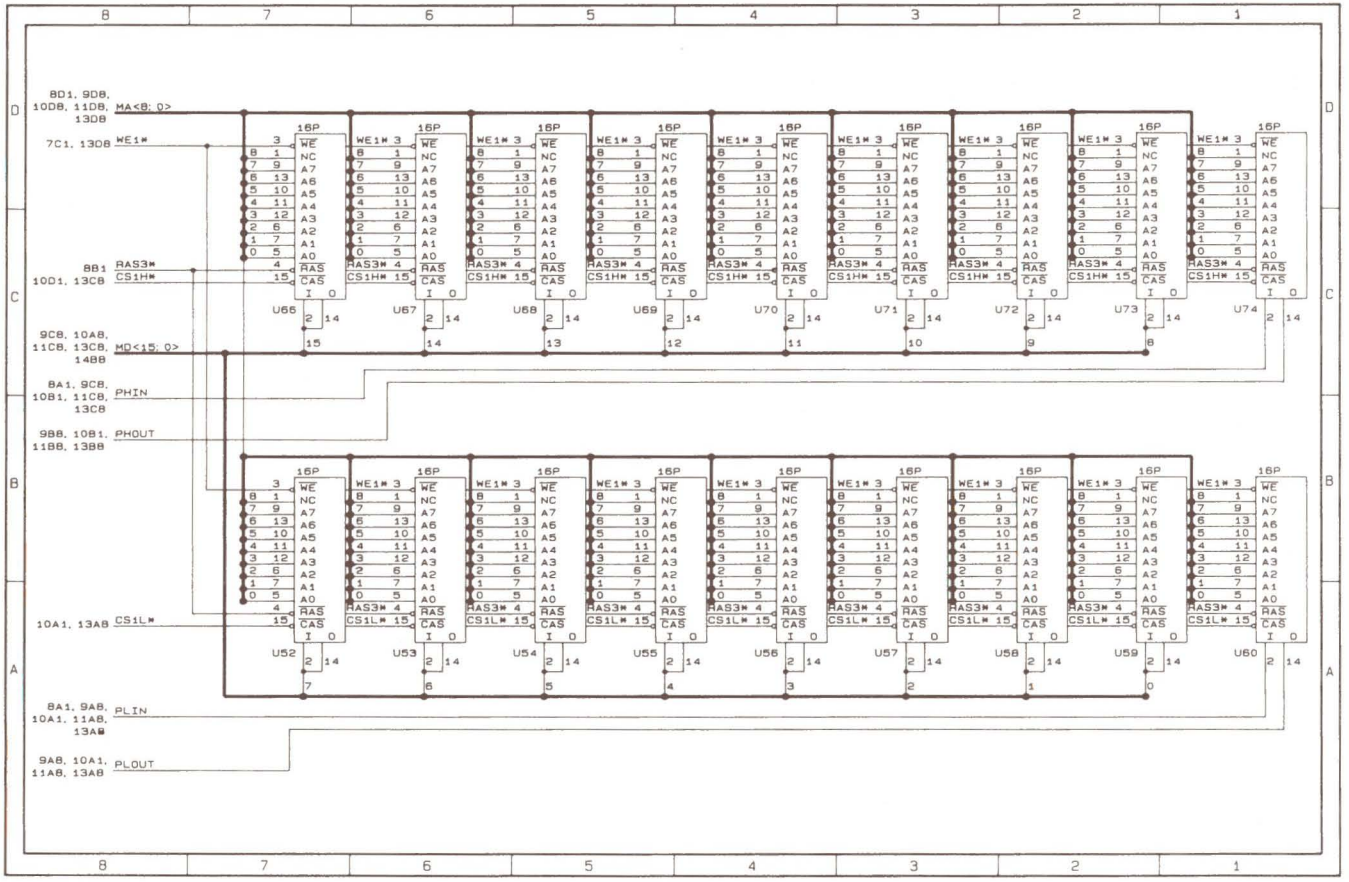


Figure 2-45. COMPAQ DESKPRO 286 Version 2 System Board Schematics (Page 12 of 18)

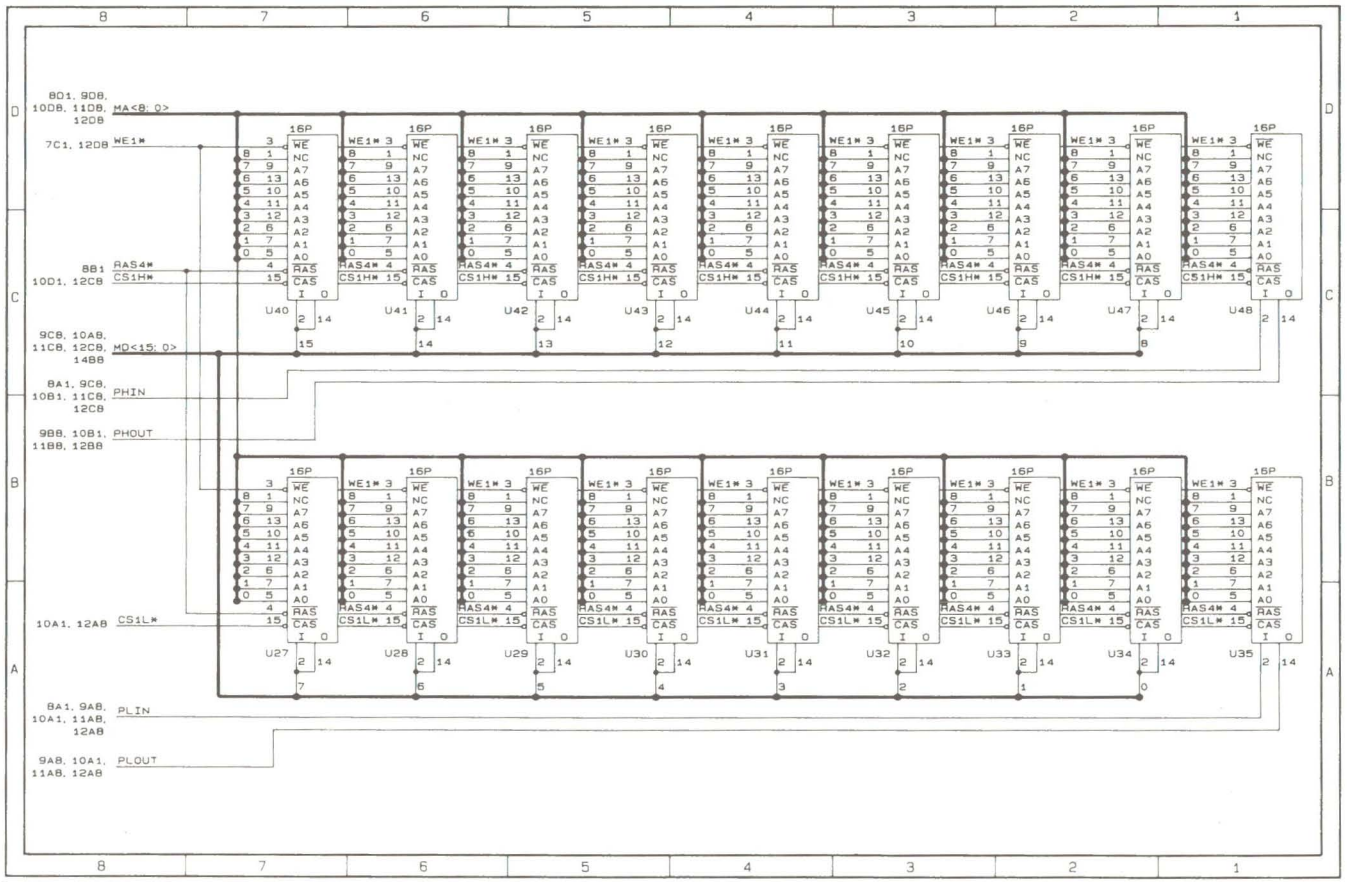


Figure 2-45. COMPAQ DESKPRO 286 Version 2 System Board Schematics (Page 13 of 18)

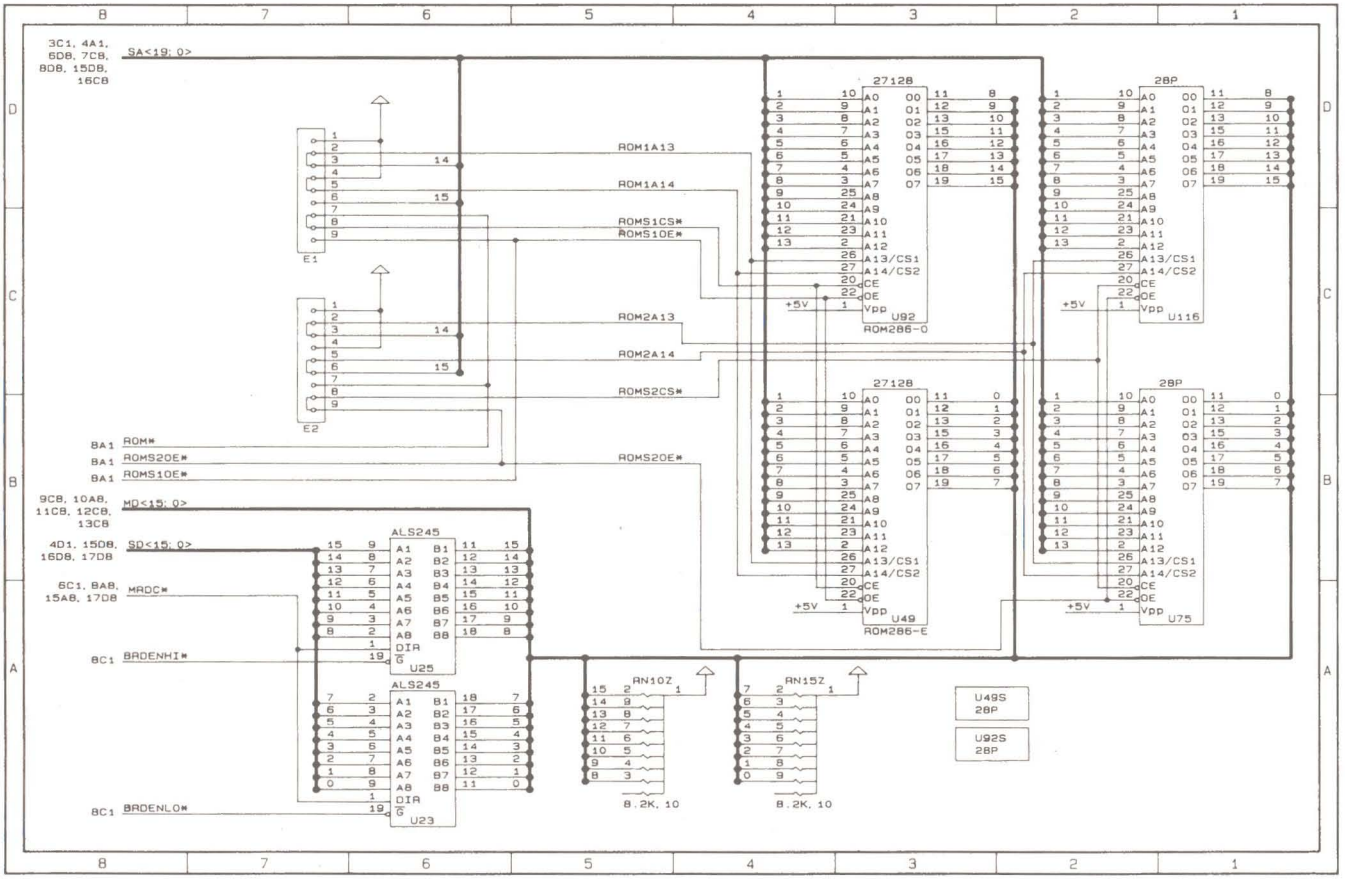


Figure 2-45. COMPAQ DESKPRO 286 Version 2 System Board Schematics (Page 14 of 18)

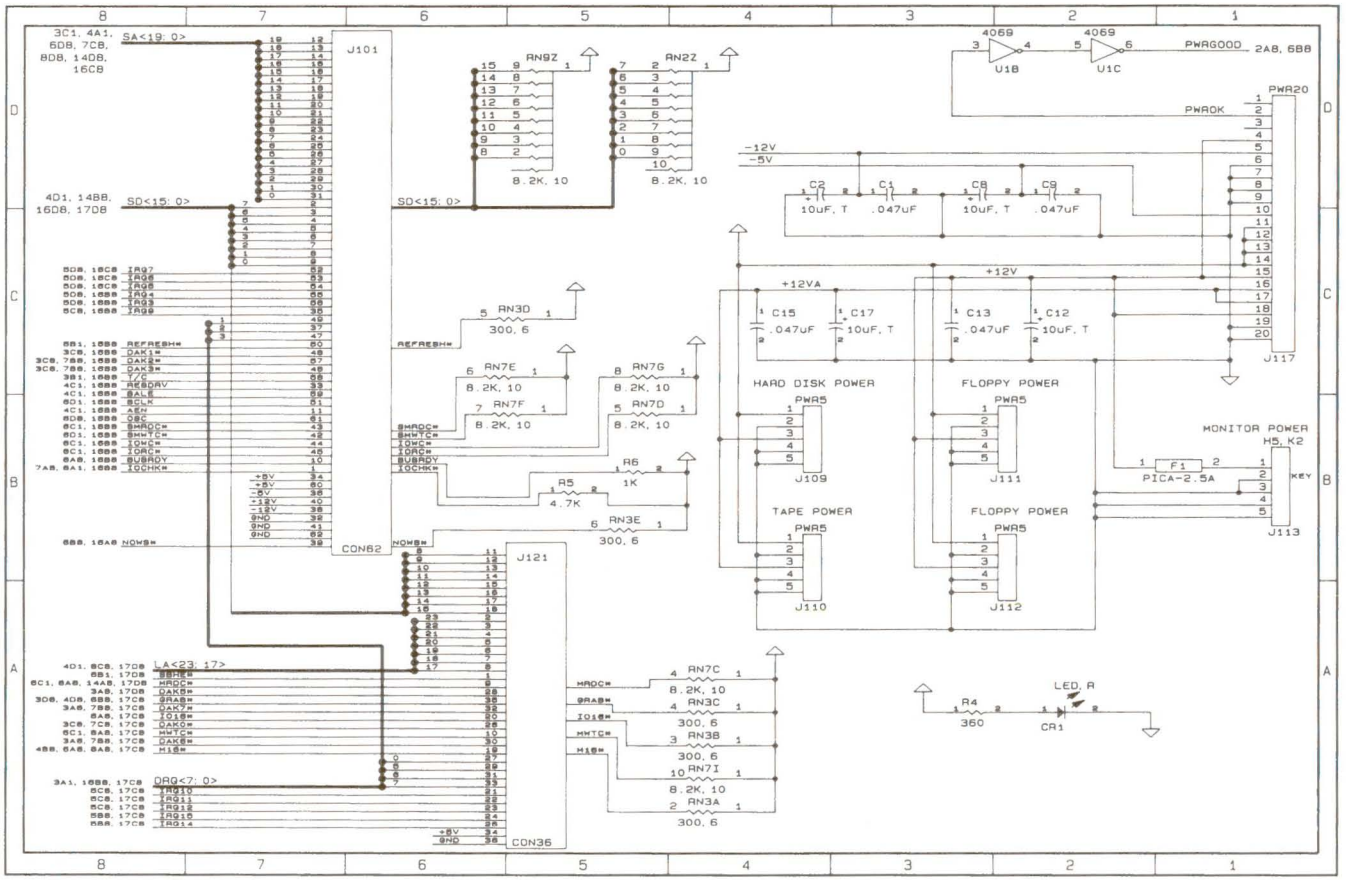


Figure 2-45. COMPAQ DESKPRO 286 Version 2 System Board Schematics (Page 15 of 18)

Figure 2-45. COMPAQ DESKPRO 286 Version 2 System Board Schematics (Page 16 of 18)

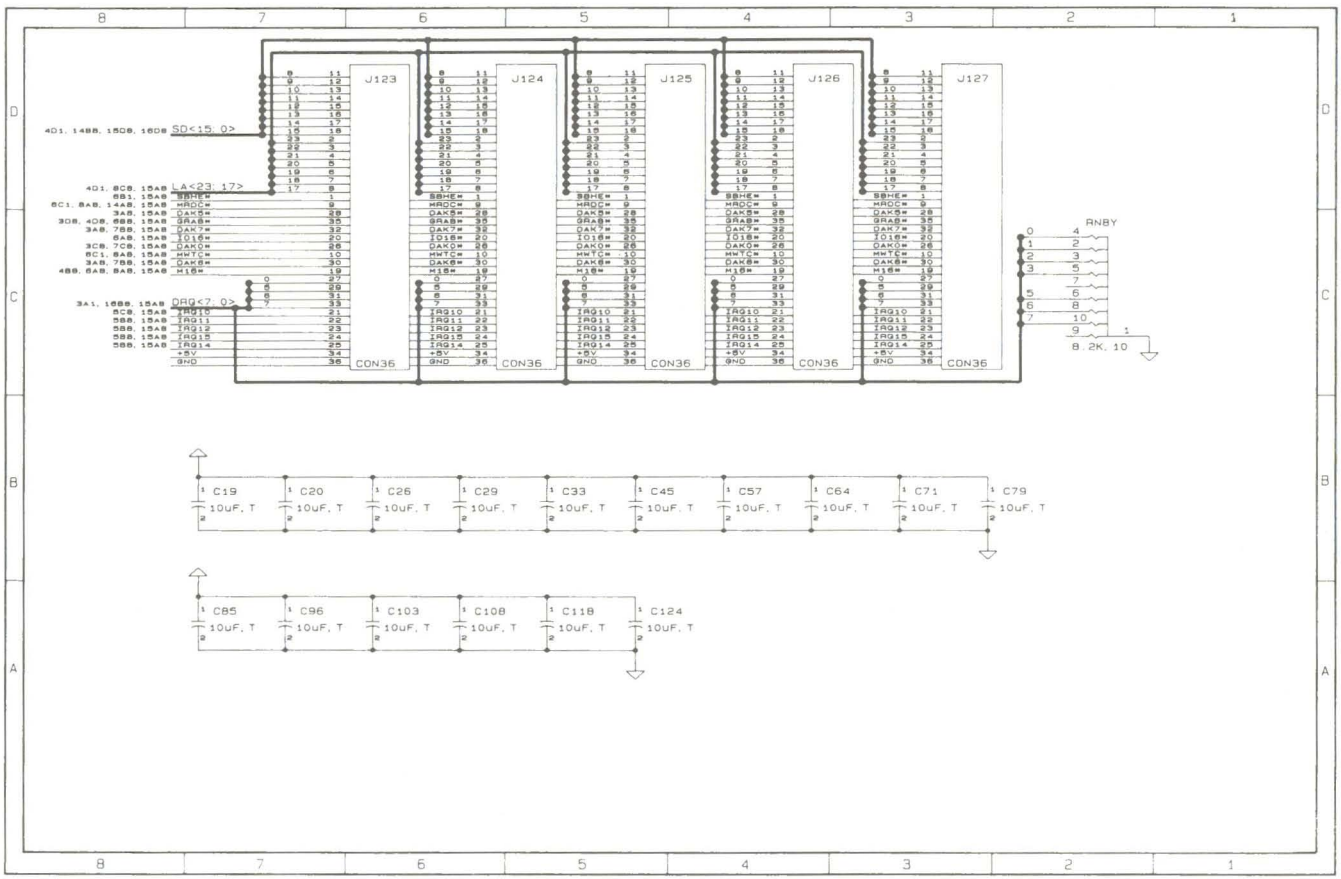


Figure 2-45. COMPAQ DESKPRO 286 Version 2 System Board Schematics (Page 17 of 18)

Figure 2-45. COMPAQ DESKPRO 286 Version 2 System Board Schematics (Page 18 of 18)

Chapter 2, Part 2

SYSTEM BOARD (12 MHz ONLY)

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CHAPTER 2, PART 2
SYSTEM BOARD (12 MHZ ONLY)

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TABLE OF CONTENTS (Continued)

2.11 THE 12 MHz COMPAQ DESKPRO 286

This chapter describes the theory of operation for the COMPAQ DESKPRO 286 Personal Computers with a 12 MHz 80286 Central Processing Unit (CPU).

Included in the description are the: CPU and CPU support circuitry, the memory system, programmable devices, and the expansion bus and bus functions as well as miscellaneous board information, jumpers, and connectors.

- CPU and CPU support circuitry, which control and monitor the system.
- Memory system, which controls access to and from the system random-access memory (RAM) and access from the system read-only memory (ROM).
- Programmable devices are hardware devices that are on the system board and that can be controlled or monitored by software.
- The expansion bus and bus functions allow system access to hardware options that may be installed in the system. Hardware options may include display controllers, communications devices, and additional memory.

Information also included in this chapter:

- Miscellaneous system board information, such as fuses and indicators
- Jumpers
- Connectors
- Schematics

Figure 2-46 is a functional block diagram of the system board.

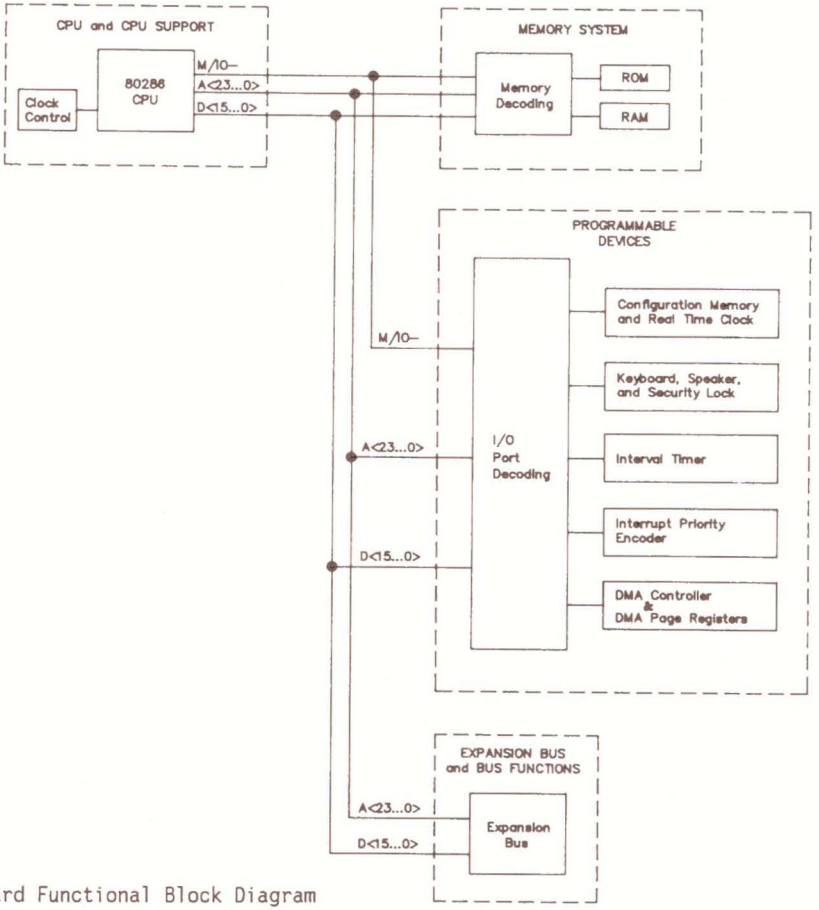


Figure 2-46. System Board Functional Block Diagram

2.12 CPU AND CPU SUPPORT

The 80286 microprocessor uses three buses, the 24-bit address bus, the 16-bit data bus, and the control bus to communicate with and control the system.

All devices outside the 80286 microprocessor are addressed either as memory-mapped devices or I/O-mapped devices.

To reset the 80286, apply power to the system board or simultaneously press the CTRL+ ALT+ DEL keys. Once the CPU is reset, it addresses the ROM for instructions. The initial boot instructions in ROM check the system RAM and ROM for errors (checksums), and then initialize the system.

System initialization, or restart of the system, includes loading the desired starting values into the programmable devices, such as the keyboard controller, the video controller, the RAM, and the CPU.

After system initialization, the CPU loads the disk operating system (DOS) into memory from the diskette or fixed disk drive. The DOS is a program that manages and provides a consistent programming interface to the hardware.

Included in this category are the:

- Clock generator and READY interface
- System control circuitry
- 80287 numeric coprocessor
- Clock function

Figure 2-47 shows a functional block diagram of the CPU and CPU support circuitry.

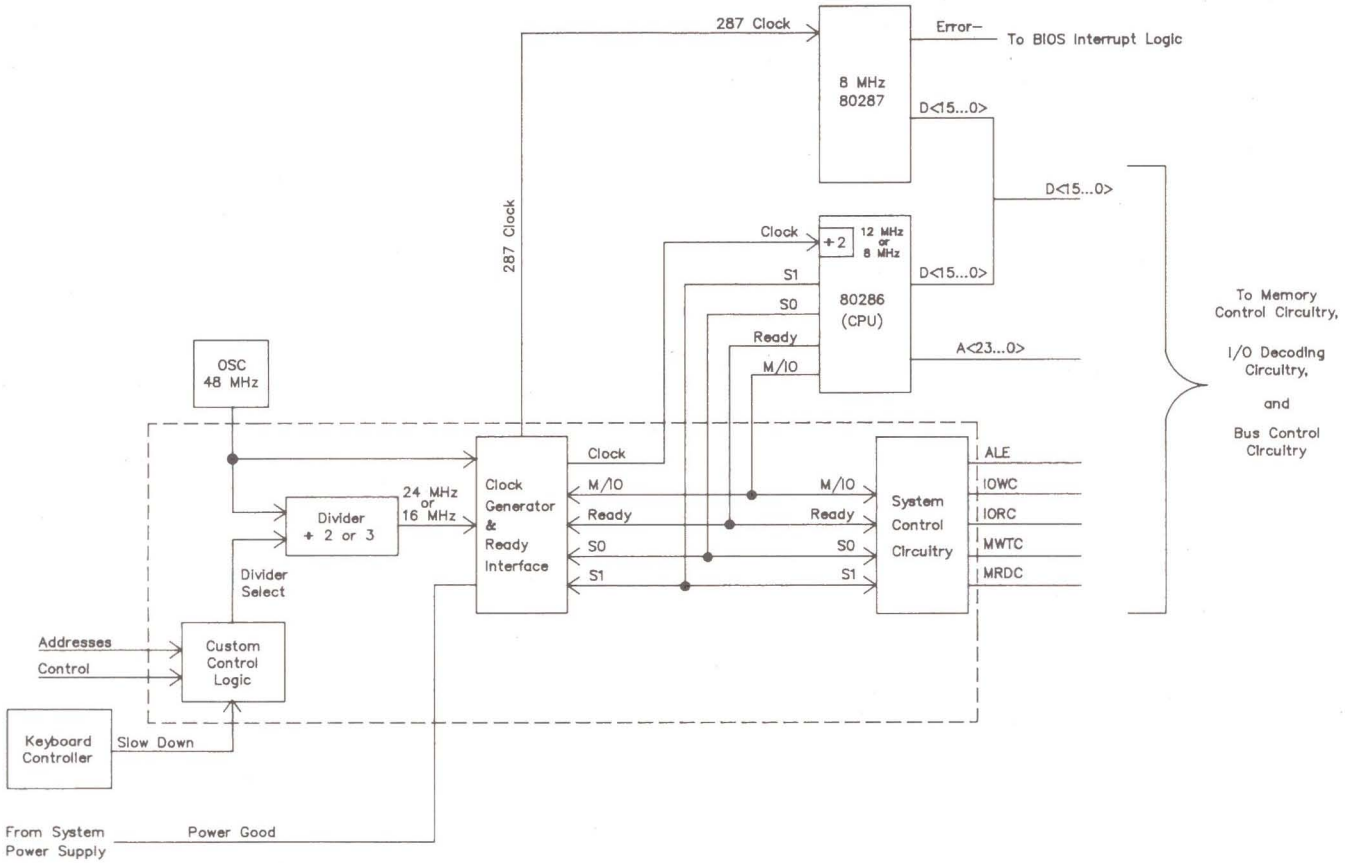


Figure 2-47. CPU and CPU Support Circuitry Block Diagram

Clock Generator and Ready Interface

The clock generator and READY interface receives an input clock signals from an oscillator circuit and generates the clock signal for the 80286 CPU, the 80287 coprocessor, and the system control circuitry. The clock generator and READY interface also monitors the power good (PWRGOOD) signal from the system power supply to control the system reset functions.

System Control Circuitry

The system control circuitry decodes the status signals S0, S1, and M/IO- (and other inputs, such as CEN/AEN, and READY-) to control the system bus.

Table 2-30 shows the bus cycle status definition for the status signals.

Table 2-30. Bus Cycle Status Definition

M/IO-	S0	S1+	Type of Bus Cycle
0	0	0	Interrupt Acknowledge
0	0	1	I/O Read (Ports)
0	1	0	I/O Write (Ports)
0	1	1	None: Idle
1	0	0	Halt or Shutdown
1	0	1	Memory Read
1	1	0	Memory Write
1	1	1	None: Idle

80287 Numeric Coprocessor (Optional)

The 80287 Numeric Coprocessor is a high-performance numeric processor extension of the 80286, adding floating-point, extended integer, and BCD data-type support.

The 80287 automatically executes all numeric instructions as they are received. The 80287 responds to particular I/O addresses (00F8h, 00FAh, and 00FCh) automatically generated by the 80286.

The 80287's ERROR- signal is connected to IRQ13 (INT 75h). The BIOS interrupt handler for INT 75h routes this interrupt to INT 02h, which is the actual routine for coprocessor exceptions. This method provides compatibility with 8088/8086-coprocessor exceptions and prevents interference with the video I/O interrupt, INT 10h.

A socket is provided on the system board for the 80287 coprocessor. The 80287 coprocessor operates at 8 MHz.

Clock Function

The COMPAQ DESKPRO 286 Personal Computer with a 12 MHz 80286 offers the choice of a 12-MHz/8-MHz switching system clock for superior processing speed or a fixed 8-MHz system clock to maintain compatibility with slower systems.

2.13 MEMORY SYSTEM

Memory Address Decoding

The 80286 uses addresses <A23..A0> and control line M/IO- to specify memory locations. The address and control lines are decoded to specify memory areas for the system RAM and ROM

The memory system includes:

- Memory address decoding
- Memory support
- Memory system (RAM & ROM)

Expansion boards such as memory, disk, or video must have their own devices to decode the I/O or memory space for that board.

Figure 2-48 shows a simplified block diagram of memory address decoding for the system board.

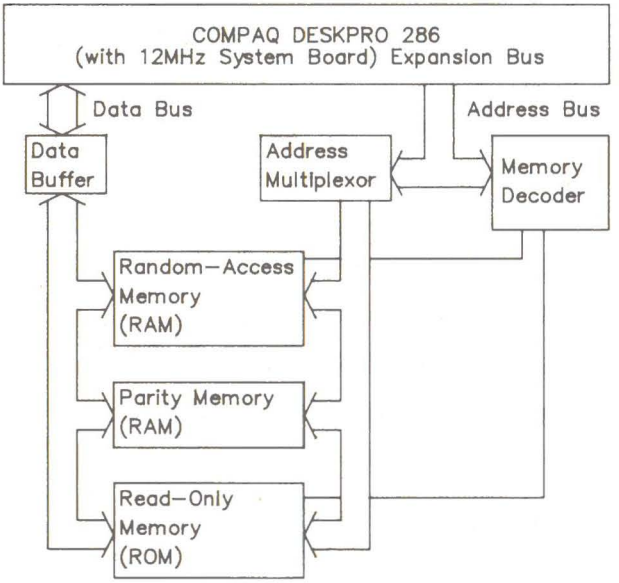


Figure 2-48. Memory Address Decoding Simplified Block Diagram

The memory decoder uses the REFRESH-, MRDC-, MWTC-, BALE, and address lines LA23 through LA17 to generate the MEM16-, RAM-, ROM-, RAS-, and CAS- signals.

The 16-bit 80286 microprocessor can read data from memory as bytes (8 bits) or words (16 bits). When it reads a word on an an even boundary, an even-numbered address is generated, and the CPU simultaneously reads that address and the one above it (Figure 2-49).

Odd-numbered, High-order Byte	Even-numbered, Low-order Byte
Byte FFFFh (64K)	Byte FFFEh (64K-1)
.	.
.	.
.	.
Byte 0003h	Byte 0002h
Byte 0001h	Byte 0000h

Figure 2-49. A 16-Bit Word Divided into Two Bytes

Two CPU cycles are required to read a word on an odd boundary. The next lower even-numbered address is first given by the CPU, and the high-order byte of that location becomes the low-order 8 bits of the word. Then, the next higher even-numbered address is given by the CPU, and the low-order byte of that location becomes the high-order 8 bits of the word.

Memory Support

Dynamic memory devices (RAM) require support circuitry to:

- Control the devices, using the CAS-, RAS-, and WR- signals
- Multiplex the address lines into the RAM
- Buffer the data lines
- Refresh the memory cells

The delay line generates the ENDRAS and STARTCAS signals and the signals that control the address multiplexing.

Three AM2966 devices buffer the address lines and sequentially present the high- and low-order address lines to the RAM. The delay line controls the timing for this multiplexing operation.

Two 74F245 chips buffer the data between the RAM and the data bus.

Memory refresh is controlled by the CBC and MSC gate arrays. During memory refresh, every cell of every memory location is recharged.

Memory System

The COMPAQ DESKPRO 286, 12 MHz version, has five banks for RAM, two 16K x 8-bit system ROMS, and two sockets for additional ROM.

Random Access Memory (RAM)

The COMPAQ DESKPRO 286, 12 MHz version, has 128 Kbytes of RAM soldered in the first bank (Bank 0). The four remaining banks (Banks 1 through 4) are socketed so that either 64K x 1-bit or 256K x 1-bit RAMS may be used. Memory must be expanded in full-bank increments (18 RAMdevices) in contiguous and ascending order, using the same RAM type (64K or 256K).

SW1 position 1 indicates the type of RAM in banks 1 through 4. When banks 1 through 4 are filled with 64K x 1-bit RAMS, SW1 position 1 must be CLOSED. When banks 1 through 4 are filled with 256K x 1-bit RAMS, SW1 position 1 must be OPEN.

NOTE: When SW1 position 1 is closed, positions 4 and 5 must both be open.

SW1 positions 2 and 3 limit the amount of base memory on the system board so that conflicts with expansion memory boards can be avoided. These two switches limit memory, as given in Table 2-31, regardless of the type of RAM in banks 1 through 4.

Table 2-31. Base Memory Size Switch (SW1) Settings

SW1		Total	Address
Position 2	Position 3	Base Memory (Note)	Ranges
CLOSED	CLOSED	Disabled RAM and ROM on System Board	
CLOSED	OPEN	256k	0-256 KB
OPEN	CLOSED	512k	0-512 KB
OPEN	OPEN	640k	0-640 KB

Legend: Closed = ON
Open = OFF

Note: Total base memory indicates maximum addressable base memory on the system board regardless of amount of RAM installed.

SW1 positions 4 and 5 enable/disable banks 2 through 4. These switches should be used to limit the amount of expansion memory on the system board when 256K x 1-bit RAMS are used to fill banks 1 through 4. Table 2-32 gives the switch settings for expansion memory.

Table 2-32. Expansion Memory Size Switch (SWI) Settings

SWI		Banks	Total Expansion Memory	Address
Position 4	Position 5	Enabled	(Note 1)	Range
CLOSED	CLOSED	None	None	-
CLOSED	OPEN	2	512K	1.0-1.5 MB
OPEN	CLOSED	2,3	1024K	1.0-2.0 MB
OPEN	OPEN	2,3,4	1536K	1.0-2.5 MB

Legend: CLOSED = ON
OPEN = OFF

Notes: 1. Total expansion memory indicates maximum addressable expansion memory on the system board regardless of amount of RAM installed.

2. SW1 positions 4 and 5 should both be OPEN when 64K x 1-bit RAMS fill banks 1 through 4 to ensure that SW1 positions 2 and 3 operate correctly.

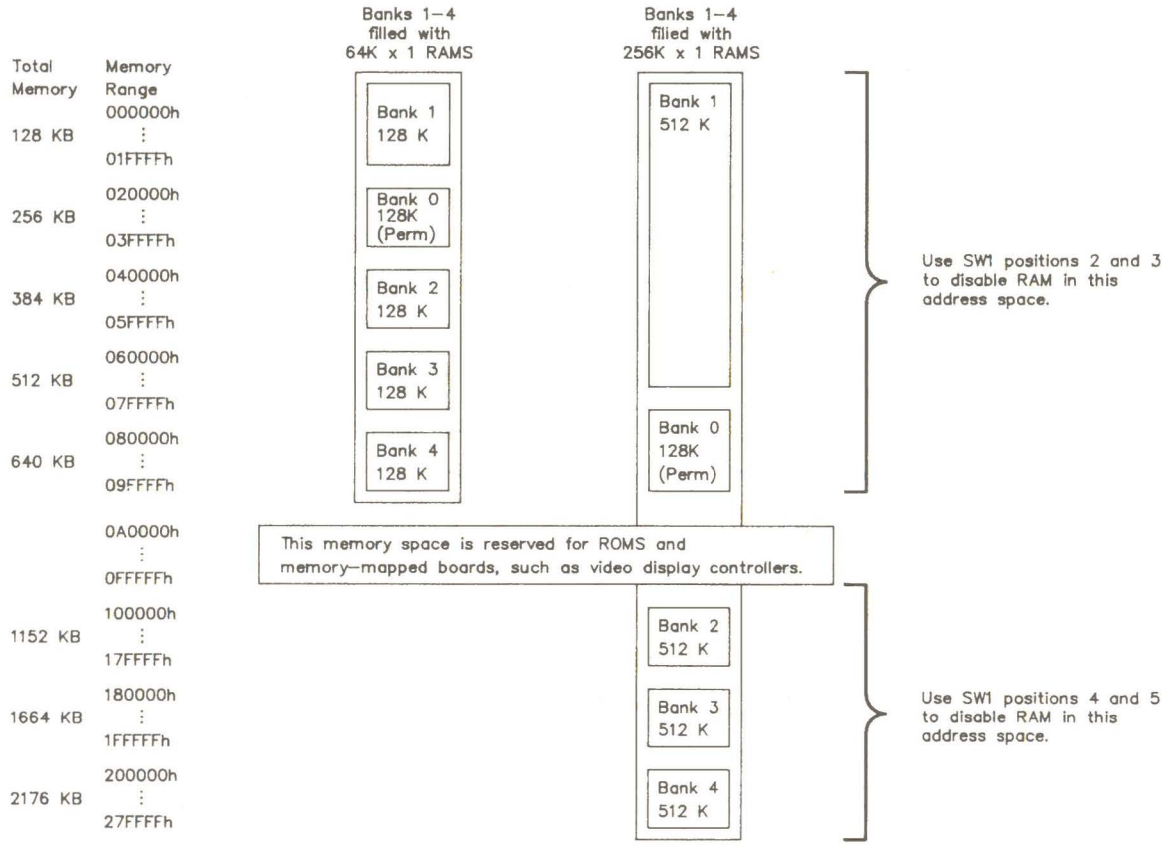


Figure 2-50. System Board Memory Configurations

The system board uses COMPAQ-approved 64K x 1-bit or 256K x 1-bit dynamic RAM devices with a response time of 100 ns or faster. (CAS access time must be 50 ns or faster.)

Read Only Memory (ROM)

The system board has four 28-pin sockets for ROM or EPROM. The ROM sockets are addressed as two pairs, each 16 bits wide and designated as ROM Set 1 (always present and including address 0FFFF0h or FFFFF0h) and system ROM SET 2 (located in the address space 64 KB below ROM Set 1).

ROM Set 1 controls the initial system operation (resetting and initializing the system). This code is known as the BIOS (basic input output system). Installed in the two ROM Set 1 sockets are 16K x 8-bit devices, one containing all even bytes and the other containing all odd bytes. The two ROM Set 2 sockets are empty and are provided for future expansion.

ROMs can be, by pairs, either 8K, 16K, or 32K x 8 bits in size and can be either static or dynamic. ROM Set 1 occupies the 64-Kbyte space at address 0F0000h through 0FFFFFh and identically at address FF0000h through FFFFFFh. ROM Set 2 occupies the 64-Kbyte space at address 0E0000h through 0EFFFFh and identically at address FE0000h through FEFFFFh.

When 32K x 8-bit ROMs are used, the pair of ROMs fill the entire 64-Kbyte address space. When 16K x 8-bit ROMs are used, the most-significant address bit is not decoded, so the ROMs are double-mapped into two identical 32-Kbyte sections of the 64-Kbyte address space.

Similarly, when 8K x 8-bit ROMs are used, the two most-significant address bits are not decoded, so the ROMs are quadruple-mapped into four identical 16-Kbyte sections of the 64 KB address space.

Jumpers

Two jumpers (E1 and E2) are provided to enable use of a variety of types of ROM for special applications.

Table 2-33 gives the jumper settings and resulting configuration for each type of ROM.

Table 2-33. Jumper Settings for ROM Sets 1 and 2

ROM Set 1 = E1
ROM Set 2 = E2

Jumper Settings			ROM Type
1-2	4-5	7-8	8K x 8, Static ROM, 150 ns
2-3	4-5	7-8	16K x 8, Static ROM, 150 ns
1-2	5-6	7-8	Invalid
2-3	5-6	7-8	32K x 8, Static ROM, 150 ns
1-2	4-5	8-9	8K x 8, Dynamic ROM, 150 ns
2-3	4-5	8-9	16K x 8, Dynamic ROM, 150 ns
1-2	5-6	8-9	Invalid
2-3	5-6	8-9	32K x 8, Dynamic ROM, 150 ns

No jumper headers are installed. The jumpers are etched on the solder side (bottom) of the board in the following configurations:

ROM Set 1:16K x 8-bit Static ROM (E1: 2-3, 4-5, 7-8)

ROM Set 2:32K x 8-bit Dynamic ROM (E2: 2-3, 5-6, 8-9)

Changing the jumper settings requires cutting the conductor on the solder side (bottom) of the board to disconnect any unwanted jumpers, then soldering wire(s) to jumpers as desired.

NOTE: Modifying these jumpers invalidates the COMPAQ warranty for this board.

2.14 PROGRAMMABLE DEVICES

The system BIOS controls the following system board programmable devices:

- Direct memory access (DMA) controllers
- DMA memory page register
- Real-time clock and configuration memory
- Keyboard controller
- Interval timer
- Interrupt priority encoder

These devices are all I/O mapped. Commands and opcodes are directed to the appropriate device by the I/O port decoding circuitry. Table 2-34 summarizes the port addresses used by the devices on the system board.

Table 2-34. System Board I/O Map

	Address Bits										
Port	9	8	7	6	5	4	3	2	1	0	Device
00h..0Fh	0	0	0	0	0	X	Y	Y	Y	Y	8237A-5 Byte DMA Controller
20h..21h	0	0	0	0	1	X	X	X	X	Y	8259A Interrupt Controller 1
40h	0	0	0	1	0	X	X	X	0	0	8254-2 System Clock (Timer 0)
41h	0	0	0	1	0	X	X	X	0	1	8254-2 Refresh Request (Timer 1)
42h	0	0	0	1	0	X	X	X	1	0	8254-2 Speaker Tone (Timer 2)
43h	0	0	0	1	0	X	X	X	1	1	8254-2 Command Mode Register
60h	0	0	0	1	1	0	X	0	X	0	8042 Date I/O Register
61h	0	0	0	1	1	0	X	X	X	1	Port B/C Input/Outputs
64h	0	0	0	1	1	0	X	1	X	0	8042 Status/Command Register
70h	0	0	0	1	1	1	X	X	X	0	RTC Address Register (Bits <5..0>)
70h	0	0	0	1	1	1	X	X	X	0	NMI Enable Register (Bit <7>)
71h	0	0	0	1	1	1	X	X	X	1	RTC Data I/O Register
80h	0	0	1	0	0	X	0	0	0	0	DMA Page Register Spare
81h	0	0	1	0	0	X	0	0	0	1	DMA Page Register CH 2 Page
82h	0	0	1	0	0	X	0	0	1	0	DMA Page Register CH 3 Page
83h	0	0	1	0	0	X	0	0	1	1	DMA Page Register CH 1 Page
84h	0	0	1	0	0	X	0	1	0	0	DMA Page Register Spare
85h	0	0	1	0	0	X	0	1	0	1	DMA Page Register Spare
86h	0	0	1	0	0	X	0	1	1	0	DMA Page Register Spare
87h	0	0	1	0	0	X	0	1	1	1	DMA Page Register CH 0 Page
88h	0	0	1	0	0	X	1	0	0	0	DMA Page Register Spare

(Continued)

Table 2-34. (Continued)

Port	Address Bits 9 8	7 6 5 4	3 2 1 0	Device
89h	0 0	1 0 0 X	1 0 0 1	DMA Page Register CH 6 Page
8Ah	0 0	1 0 0 X	1 0 1 0	DMA Page Register CH 7 Page
8Bh	0 0	1 0 0 X	1 0 1 1	DMA Page Register CH 5 Page
8Ch	0 0	1 0 0 X	1 1 0 0	DMA Page Register Spare
8Dh	0 0	1 0 0 X	1 1 0 1	DMA Page Register Spare
8Eh	0 0	1 0 0 X	1 1 1 0	DMA Page Register Spare
8Fh	0 0	1 0 0 X	1 1 1 1	DMA Page Register Refresh Page
A0h..A1h	0 0	1 0 1 X	X X X Y	8259A Interrupt Controller 2
C0h..CFh	0 0	1 1 0 Y	Y Y Y X	8237A-5 Word DMA Controller
F0h	0 0	1 1 1 X	0 X X 0	Clear Numeric Processor Busy
F1h	0 0	1 1 1 x	0 X X 1	Reset Numeric Processor
F8h..FFh	0 0	1 1 1 1	1 Y Y X	80287 Command Ports

Legend: X = Don't care. The value of these bits does not affect the I/O address decoding.
Y = Register dependent.

I/O Port Decoding

The 80286 uses address (A<15...0>) and control lines (M/IO-) to specify I/O operations. Although the 80286 uses 16 bits for an I/O address, the system board and expansion boards use only 10 bits (A<9...0>), therefore I/O space is limited to 3FFh. The address and control lines are decoded to provide chip selects and addresses for the system board I/O-mapped devices (DMA controllers, real-time clock, and interval timer).

Each expansion board such as memory, disk, and video, must have its own device to decode the I/O-mapped devices for that board. Figure 2-51 shows a simplified block diagram of I/O port decoding for the system board.

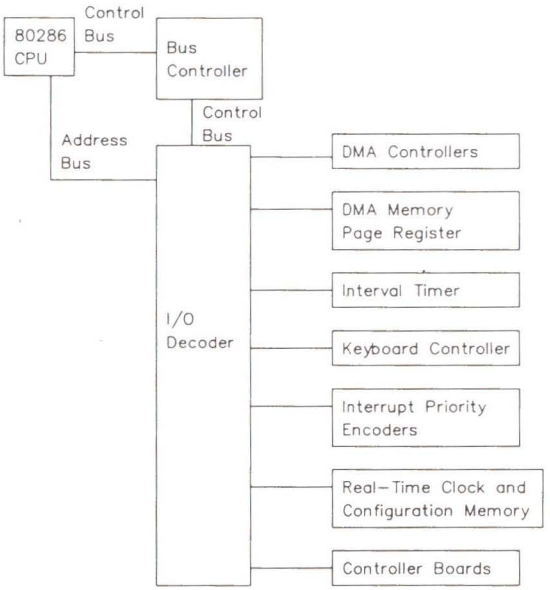


Figure 2-51. I/O Address Decoding Simplified Block Diagram

Direct Memory Access Controllers

Direct memory access (DMA) is a method of directly accessing memory without involving the CPU. DMA is normally used to transfer blocks of data to or from an I/O device. DMA reduces the amount of CPU interactions with memory, freeing the CPU for other processing tasks.

The system board uses two Intel 8237 DMA controllers; with four bidirectional data channels each. The DMA controllers operate at 4 MHz. Table 2-35 lists the function assigned to each DMA channel.

Table 2-35. DMA Channels Assigned to the Controllers

Channel	Function
Controller 1 (Byte Transfers)	
0	Spare
1	SDLC (Communications)
2	Diskette Data Transfers
3	Spare
Controller 2 (Word Transfers)	
4	Cascade for Controller 1
5	Spare
6	Spare
7	Spare

The DMA controllers hold (or define) only 16 bits of the 24-bit address. The other 8 address bits are generated by the MAP gate array. See the "DMA Memory Page register" section for more information.

DMA Controller 1 is used for byte (8-bit) data transfers. DMA Controller 2 is used for word (16-bit) data transfers. Unlike the CPU, DMA Controller 2 can only transfer words on an even boundary. Figure 2-52 shows memory address derived from page register and DMA register contents.

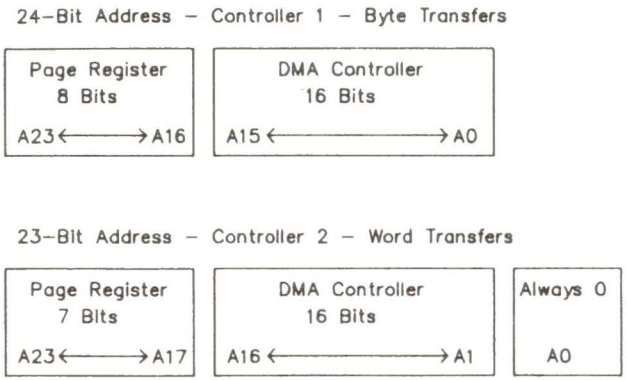


Figure 2-52. Memory Address Derived from Page Register and DMA Register Contents

A16 from the DMA memory page register is disabled when DMA Controller 2 is selected. A0 is not connected to DMA Controller 2. A0 is always 0 when word-length transfers are selected. This arrangement (not connecting A0) means that the size of the block of data that can be moved or addressed is measured in 16-bit words, rather than 8-bit bytes.

Since the DMA controllers only contain 16 bits of the 24-bit address, they can move blocks of data only within their ability to address that data.
DMA Controller 1 can move up to 64-Kbytes of data.
DMA Controller 2 can move up to 64K words, or 128-Kbytes of data.

The DMA controllers are complex devices with several registers for commands and status. Table 2-36 lists the I/O map and the commands and formats of the registers.

Transferring Data from I/O Devices to Memory

DMA controllers and I/O devices use the DRQx and DAKx signals as "handshaking". When an I/O device has a byte or word of data to send, the I/O device makes its DRQx line active. When the DAKx line from the DMA controller goes active, the device puts its data on the data bus.

Transferring Data from Memory to Memory

The hardware does not support memory-to-memory block transfers.

NOTE: After power-on, it is recommended that all Command, Mode, and Mask registers be loaded with valid values to ensure proper operation of the device.

Table 2-36. DMA Controller Registers

Register Function	Bits	Port Addresses Cntlr 1	Cntlr 2	Read/Write
Status	8	08h	D0h	Read
Command	8	08h	D0h	Write
Mode	6	0Bh	D6h	Write
Write Single Mask Bit	4	0Ah	D4h	Write
Write All Mask Bits	4	0Fh	DEh	Write
Software DRQx Request	4	09h	D2h	Write
Base and Current Address - CH 0	16	00h	C0h	Write
Current Address - CH 0	16	00h	C0h	Read
Base and Current Word Count - CH 0	16	01h	C2h	Write
Current Word Count - CH 0	16	01h	C2h	Read
Base and Current Address - CH 1	16	02h	C4h	Write
Current Address - CH 1	16	02h	C4h	Read
Base and Current Word Count - CH 1	16	03h	C6h	Write
Current Word Count - CH 1	16	03h	C6h	Read
Base and Current Address - CH 2	16	04h	C8h	Write
Current Address - CH 2	16	04h	C8h	Read
Base and Current Word Count - CH 2	16	05h	CAh	Write
Current Word Count - CH 2	16	05h	CAh	Read
Base and Current Address - CH 3	16	06h	CCh	Write
Current Address - CH 3	16	06h	CCh	Read
Base and Current Word Count - CH 3	16	07h	CEh	Write

(Continued)

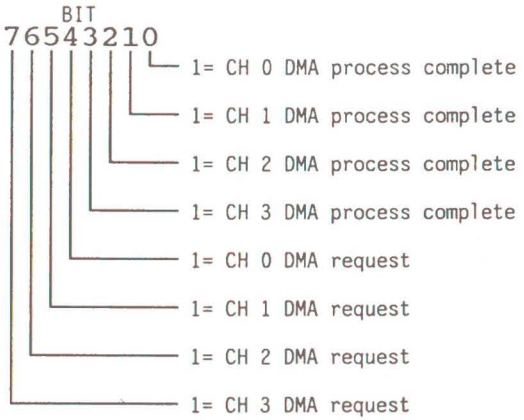
Table 2-36. (Continued)

Register Function	Bits	Port Addresses Cntrl 1	Cntrl 2	Read/Write
Current Word Count - CH 3	16	07h	CEh	Read
Temporary	16	0Dh	DAh	Read
Reset Pointer Flip-flop	(Notes 1,2)	0Ch	D8h	Write
Master Reset	(Note 2)	0Dh	DAh	Write
Reset Mask Register	(Note 2)	0Eh	DCh	Write

Notes: 1. See "RESET POINTER FLIP-FLOP" for an explanation of 16-bit data transfers to the DMA controllers.
2. This is not a register, but a direct command to the DMA Controller.

STATUS

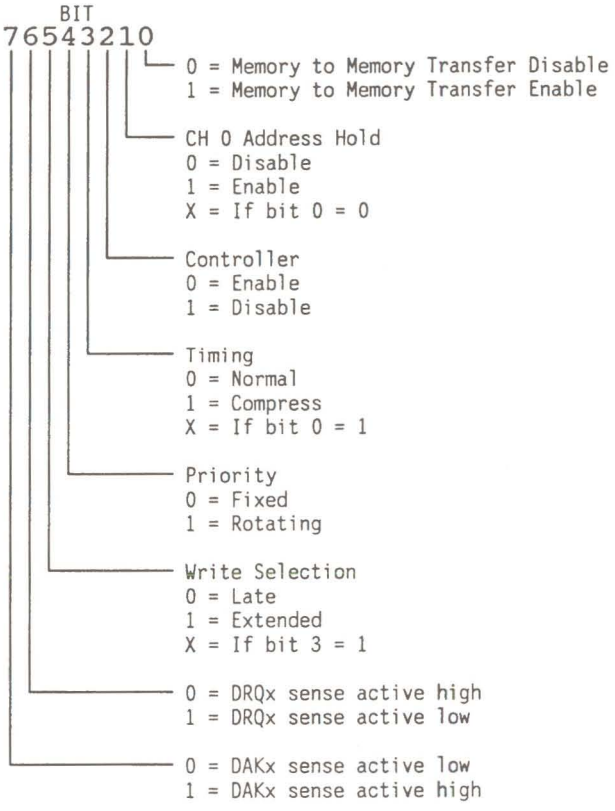
The Status register bits are set (= 1) to indicate that a channel has requested DMA access or that a DMA process is complete.



COMMAND

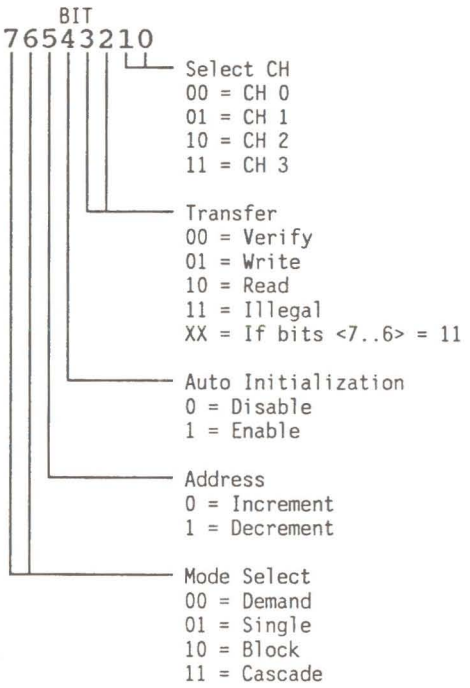
The Command register bits control the DMA operation. All bits are reset (=0) by the master clear instruction or a system reset. This register must be programmed to 00 for proper system operation.

COMMAND (Continued)



MODE

Each channel has a 6-bit register associated with it. The first 2 bits of the byte written to this register specify which channel is being selected. These registers specify the operating mode for each channel.

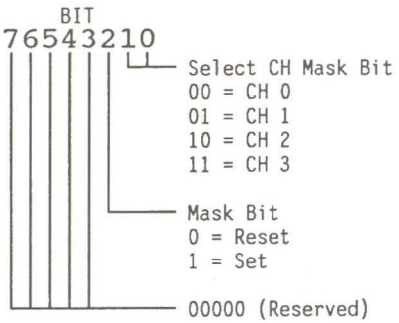


MODE (Continued)

If the Block or Demand mode is selected for a channel, the total transfer time must not exceed 15 us or RAM is not properly refreshed.

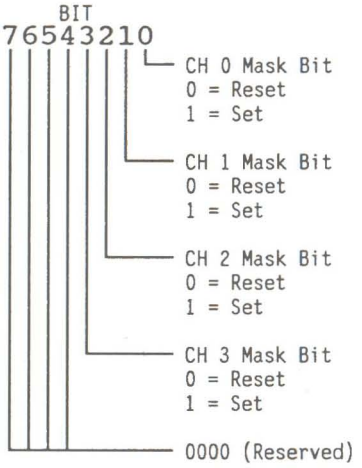
WRITE SINGLE MASK BIT

This command sets (=1) or resets (=0) a single mask bit. When a mask bit is set, that channel's DRQx is disabled. The "WRITE ALL MASK BITS" command can set or reset all the mask bits.



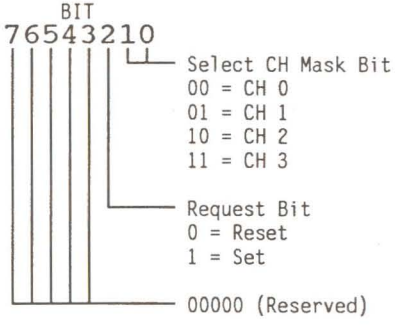
WRITE ALL MASK BITS

This command sets (=1) or resets (=0) all the Mask bits. When a bit is set, that channel's DRQx is disabled. The "WRITE SINGLE MASK BIT" command can set or reset a single mask bit.



SOFTWARE DRQx REQUEST

The DMA controller can respond to software requests for DMA as well as hardware requests from DRQx lines. The channel must be in the block mode, and the appropriate registers (base addresses and so forth) must be set before initiating this request.



BASE AND CURRENT ADDRESS - CHANNELS 0-3

These 16-bit registers specify the starting destination address for the memory transfer. This is a write-only register. The 16-bit contents are loaded into these registers as a two-part operation. The first write to this register loads the 8 least-significant bits. The second consecutive write loads the 8 most-significant bits. See the "RESET POINTER FLIP-FLOP" command.

CURRENT ADDRESS-CHANNELS 0-3

These 16-bit registers specify either the current address or the destination address for the next data transfer. This address is the same as the base address, plus address increments or decrements made after each data transfer. These are read-only registers. The 16-bit contents are read from these registers as a two-part operation. The first read from this register returns the 8 least-significant bits. The second consecutive read returns the 8 most-significant bits. See the "RESET POINTER FLIP-FLOP" command.

BASE AND CURRENT WORD COUNT - CHANNELS 0-3

These 16-bit registers specify the number of words to be transferred. This is a write-only register. The 16-bit contents are loaded into these registers as a two-part operation.

The first write to this register loads the 8 least-significant bits. The second consecutive write loads the 8 most-significant bits. See the "RESET POINTER FLIP-FLOP" command, (QF12).

CURRENT WORD COUNT - CHANNELS 0-3

These 16-bit registers specify the number of words already moved as part of a data block. These are read-only registers. The 16-bit contents are read from these registers as a two-part operation. The first read from this register returns the 8 least-significant bits. The second consecutive read returns the 8 most-significant bits. See the "RESET POINTER FLIP-FLOP" command.

TEMPORARY

This register is not used in this hardware configuration.

RESET POINTER FLIP-FLOP

This is a direct command to the DMA controller to reset the pointer flip-flop that keeps track of 16-bit data transfers. This command resets the pointer to a known state so that the DMA controller can load the high- and low-order bytes in the proper sequence. Use this command before writing a 16-bit base address or other 16-bit command or data to the DMA controller.

MASTER RESET

This is a direct command to the DMA controller to reset the DMA controller It has the same effect as a hardware reset; the Command, Status, Request, Temporary, and Pointer Flip-Flop registers are reset (=0), and the Mask register bits are set (=1).

RESET MASK

This is a direct command to the DMA controller to reset the Mask register, enabling all four channels to receive DRQs (data requests).

DMA Memory Page Register

The DMA Memory Page register contains the 8 most-significant bits of the 24-bit address. It works in conjunction with the DMA controllers to define the complete (24-bit) address for the DMA channels. Table 2-37 lists the port address assigned to each page register. For more information on the DMA controllers, see Section 2.14.

Table 2-37. Port Address For DMA Channels

DMA Channel	Page Register I/O Port Address
0	087h
1	083h
2	081h
3	082h
4	None
5	08Bh
6	089h
7	08Ah
Refresh	08Fh (See Note)

Note: The DMA Memory Page register for the refresh channel must be programmed with 00h for proper system operation.

Real-Time Clock and Configuration Memory

The COMPAQ 286 family computer system boards use the Motorola MC146818 device as their real-time clock (RTC) and configuration memory. This device has a total of 64 bytes of memory. The first 14 memory locations are used for the RTC. The remaining 50 memory locations are used for the system configuration.

A value can be written to or read from all 64 registers except:

- Status registers C and D, which are read-only
- Bit <7> of Status register A, which is read only
- The high-order bit of the seconds byte, which is read-only

Figure 2-53 shows the memory map for the MC146818.

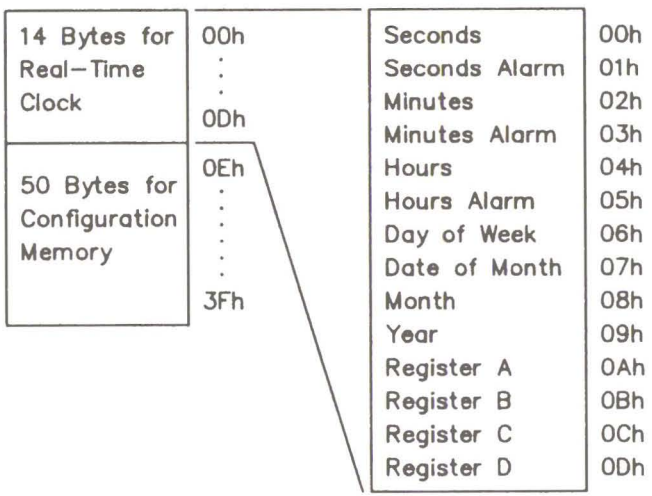


Figure 2-53. MC146818 Memory Map

To prevent a loss of time or system configuration, the MC146818 uses power obtained from a battery mounted on the inside of the computer. The battery maintains the time and system configuration during power loss for as long as three years. The system does NOT charge the battery.

NOTE: If the battery is disconnected or fails for any reason, the time and system configuration must be reprogrammed into the MC146818.

To reset the time or system configuration, run the SETUP procedure found on the USER'S PROGRAM diskette or on the Advanced Diagnostics Diskette. To reset the time, use either the SETCLOCK (DOS) command, or the appropriate INT 1Ah (BIOS) command.

The MC146818 is an I/O mapped device. Use the 80286 OUT and IN instructions to read or write to the memory in this device. Note that the port 70h is shared between the NMI Mask register and the Configuration Memory Address register. To leave the NMI Mask enabled, make sure that bit <7> is set to 0 when writing a RTC address to port 70h.

To write a value into memory:

1. Use OUT 70h, AL to specify the memory location to change. 70h is the port number; AL is the memory location.
2. Use OUT 71h, AL to specify the data for the memory location. 71h is the port number; AL is the data.

To read the contents of a memory location:

1. Use OUT 70h, AL to specify the memory location to read. 70h is the port number; AL is the memory location.
2. Use IN AL, 71h to read data stored in that location. The returned data is placed in the AL register of the 80286.

Table 2-38 summarizes the types of information stored in the MC146818's memory locations.

Table 2-38. MC146818 Real-Time Clock Memory Locations

Register	Function
00h	Seconds
01h	Seconds Alarm
02h	Minutes
03h	Minutes Alarm
04h	Hour
05h	Hour Alarm
06h	Day of Week
07h	Day of Month
08h	Month
09h	Year
0Ah	Status Register A
0Bh	Status Register B
0Ch	Status Register C
0Dh	Status Register D
0Eh	Diagnostic Register
0Fh	Reset Code Byte
10h	Diskette Drive Type
11h	Reserved
12h	Fixed Disk Drive Type
13h	Reserved
14h	Equipment Installed

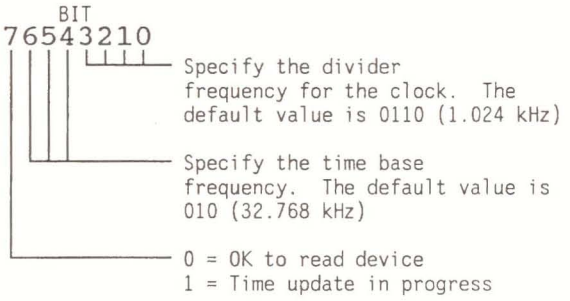
(Continued)

Table 2-38. (Continued)

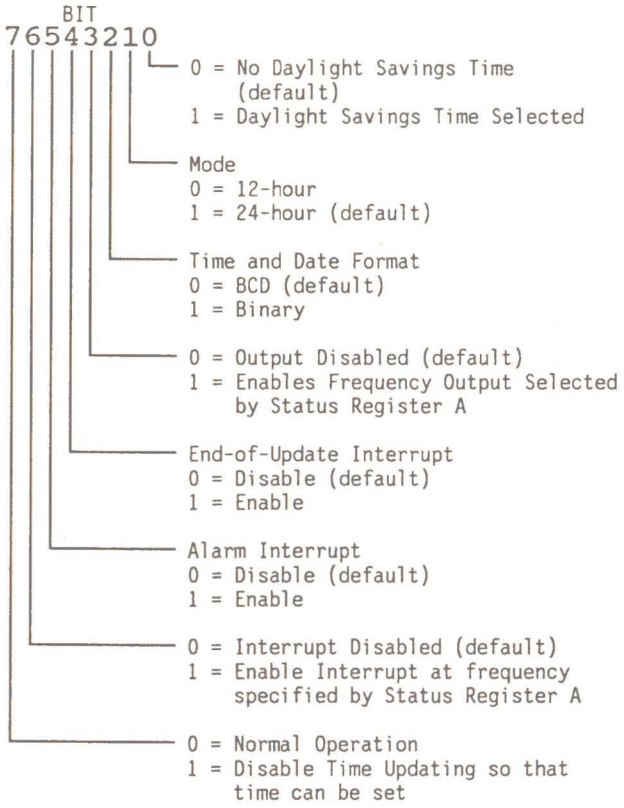
Register	Function
15h,16h	System Board Memory Size
17h,18h	Extended Memory Installed
19h-2Ch	Reserved
2Dh	Additional Flags
2Eh,2Fh	Checksum Value
30h,31h	Memory More than 1 MB
32h	Century (part of time and date function)
33h	System Information
34h-3Fh	Reserved

Information about registers 0Ah through 33h follows.

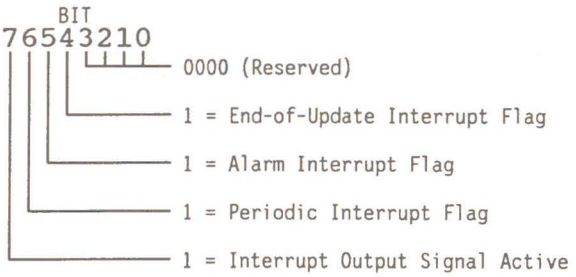
STATUS - BYTE 0Ah



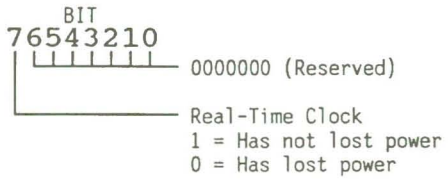
STATUS - BYTE 0Bh



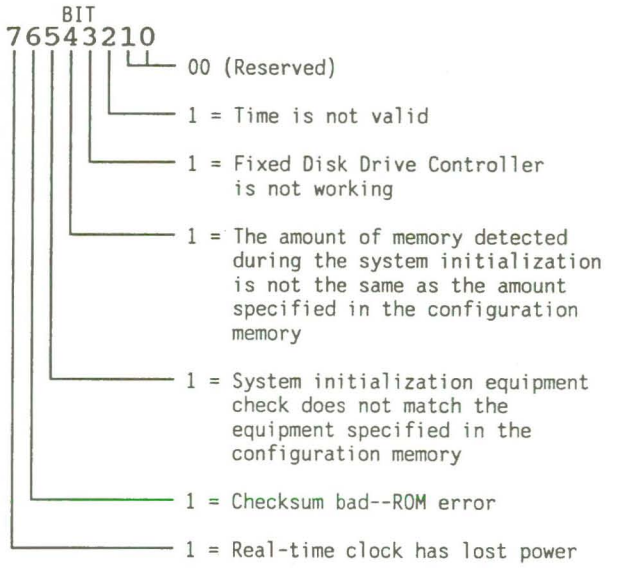
STATUS - BYTE 0Ch--READ-ONLY



STATUS - BYTE 0Dh



CONFIGURATION BYTE 0Eh--DIAGNOSTIC STATUS BYTE

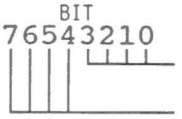


CONFIGURATION BYTE 0Fh--RESET CODE BYTE

The reset code tells the system what to do after the CPU is reset. The reset code identifies the type of, or reason for, reset. The reset code also provides a method of resetting the system without losing previously stored data or to return the system to the Real mode from the Protected Virtual Memory mode.

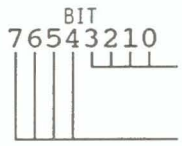
00h = Normal power-on reset
04h = Proceed to load DOS from disk
05h = Jump to Reset Vector 0040:0067 after initializing the 8259A's
09h = Block Move Return
0Ah = Jump to Reset Vector 0040:0067 after initializing the 8259A's

CONFIGURATION BYTE 10h--DISKETTE DRIVE TYPE



Secondary Diskette Drive Type
(Use values given below)
Primary Diskette Drive Type:
0000 = No diskette drive
0001 = 360-Kbyte Diskette Drive
0010 = 1.2-Megabyte Diskette Drive
0011 = Reserved
:
1111 = Reserved

CONFIGURATION BYTE 12h--FIXED DISK DRIVE TYPE



Value defines second fixed disk drive type (Use table below)

Value defines fixed disk drive type:

Value	Size	System
0000	None	- -
0010	20-MB	COMPAQ PORTABLE 286
0010	20-MB	COMPAQ DESKPRO 286
0110	30-MB	COMPAQ DESKPRO 286
1100	70-MB	COMPAQ DESKPRO 286

NOTE: This byte identifies the type of fixed disk drive used, not the capacity.

CONFIGURATION BYTE 14h--EQUIPMENT INSTALLED

Diskette Drive
0 = None installed
1 = Installed

Numeric Coprocessor
0 = None installed
1 = Installed

00 (Reserved)

Type of primary video display controller and operating mode
00 = Reserved
01 = Color/Graphics, 40 column
10 = Color/Graphics, 80 column
11 = Non-COMPAQ monochrome/text

Number of diskette drives installed
00 = 1
01 = 2
10 = Reserved
11 = Reserved

CONFIGURATION BYTES 15h AND 16h--BASE MEMORY SIZE

Value indicates valid memory sizes for the base memory size:

Byte 16h	Byte 15h	Memory Size
00h	80h	128 KB
01h	00h	256 KB
02h	00h	512 KB
02h	80h	640 KB

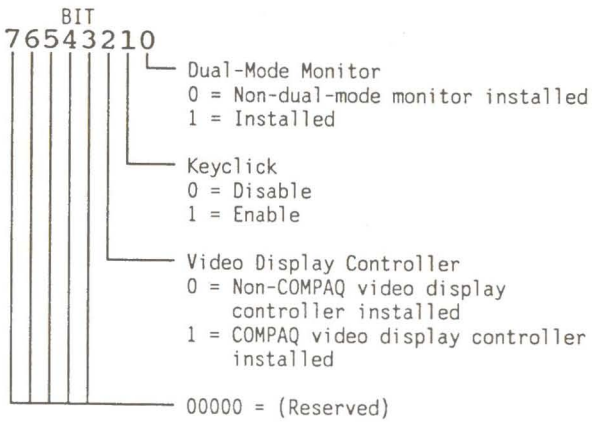
CONFIGURATION BYTES 17h AND 18h--EXPANSION MEMORY SIZE

Value indicates valid memory sizes for all expansion memory:

Byte 18h	Byte 17h	Memory Size
02h	00h	512 KB
04h	00h	1024 KB
06h	00h	1536 KB
.	.	.
.	.	.
3Bh	80h	15232 KB

CONFIGURATION BYTE 2Dh--ADDITIONAL FLAGS

This byte allows the configuration of special features.



CONFIGURATION BYTES 2Eh AND 2Fh--MEMORY CHECKSUM

Value stored is the checksum for memory addresses 10h..2Dh.

Byte 2Eh = High byte of checksum

Byte 2Fh = Low byte of checksum

CONFIGURATION BYTES 30h AND 31h--MEMORY OVER 1 MB

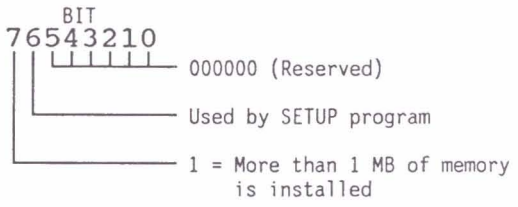
Value indicates amount of system memory in excess of 1 MB. These bytes are updated by the BIOS at power-on.

Byte 31h	Byte 30h	Memory Size
02h	00h	512 KB
04h	00h	1024 KB
06h	00h	1536 KB
08h	00h	2048 KB
0Ah	00h	2560 KB
0Ch	00h	3072 KB
0Eh	00h	3584 KB
10h	00h	4096 KB
12h	00h	4608 KB
14h	00h	5120 KB
16h	00h	5632 KB
18h	00h	6144 KB
1Ah	00h	6656 KB
1Ch	00h	7168 KB
1Eh	00h	7680 KB
.	.	.
.	.	.
3Bh	80h	15232 KB

CONFIGURATION BYTE 32h--DATE, CENTURY

This is the century part of the current time and date encoded in BCD (binary coded decimal). The BIOS sets and reads this value.

CONFIGURATION BYTE 33h--SYSTEM INFORMATION



Keyboard Controller

An INTEL 8042 single-device microcomputer provides:

- An output port for system function control and keyboard communication
- An input port to read system function status
- A test port to read the status of the keyboard clock and data lines

The 8042 has internal ROM that is custom-programmed with keyboard scan codes and operating instructions. Figure 2-54 shows a simplified block diagram of the keyboard controller.

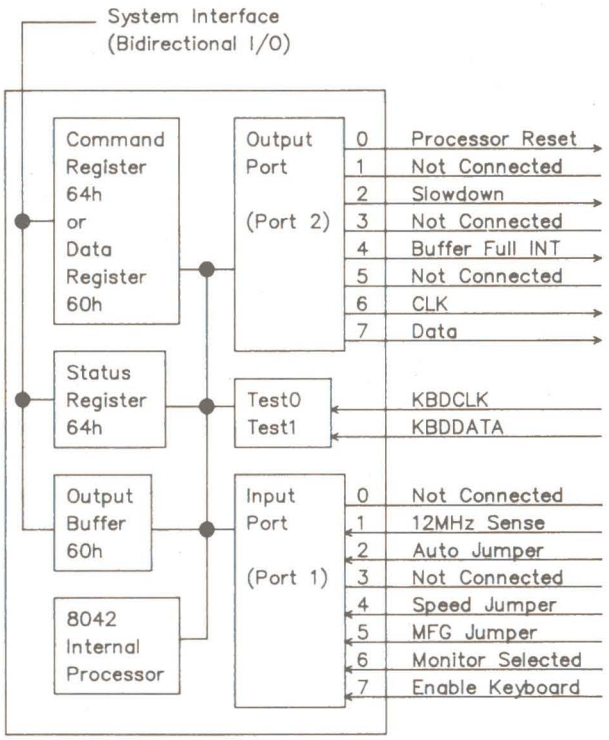


Figure 2-54. Keyboard Controller Functional Block Diagram

The 8042 communicates with the keyboard in a bidirectional, serial format with a synchronizing clock. The 8042 receives serial data, checks its parity, translates the 11- or 9-bit scan codes from the keyboard into system codes, and interrupts the 80286 to transfer data into the system.

(Command codes between the 8042 and the keyboard are described in Chapter 8.)

8042-to-Keyboard Interface

The 8042 and the keyboard are connected by a four conductor, shielded cable that carries a power line, a ground line, a Data signal, and a Clock signal.

The 8042 and the keyboard communicate in a handshaking fashion, using the Data and Clock lines for synchronous serial communication. The Data and Clock lines are driven by open-collector-type drivers at both ends of the cable in a wired-OR fashion.

The keyboard supplies the synchronizing clock for data transmissions in either direction.

Figure 2-55 shows a simplified schematic of the data and clock circuits.

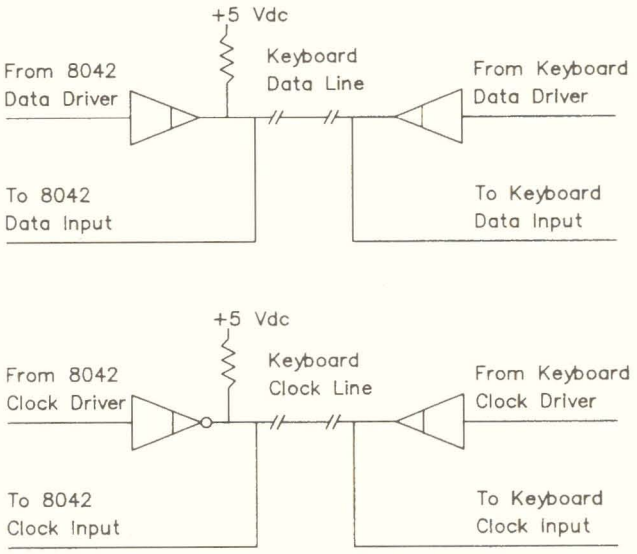
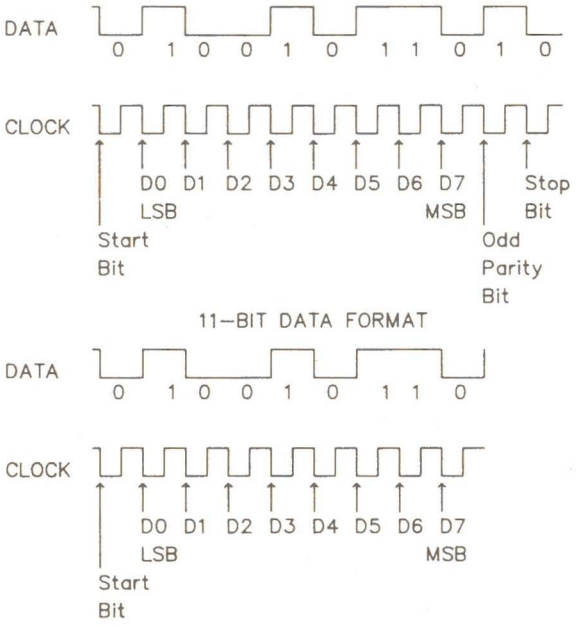


Figure 2-55. Simplified Schematic of the Data and Clock Circuits

11- or 9-Bit Data Transmission Format

The 8042 adds versatility to the system by allowing 11- or 9- bit keyboards to be used interchangeably at any time. The system sends commands to the 8042 to specify the type of scan code it expects, and the 8042 sends that type of scan code, regardless of the type of keyboard connected.

The 8042 automatically tests for keyboard type by monitoring the data format. Figure 2-56 shows 11- and 9- bit data formats with sample data transfers.



Note: The keyboard drives the data line low for the Stop Bit at the end of a transmission to acknowledge the transmission.

Figure 2-56. 11- and 9-Bit Data Formats

Table 2-39 lists the 11- and 9-bit data transfer timing parameters.

Table 2-39. Keyboard Data Timing Parameters

Parameter	11-Bit	9-Bit
Clock timing (min.), Falling edge to falling edge	60 us	25 us
Clock timing (min.), Falling edge to rising edge	5 us	5 us
Transmission Time (max.) First edge to completion	2 us	2 us
Time data must be valid before falling clock edge	0 us	0 us
Time data must be valid after falling clock edge	5 us	12 us

8042 Port Functions

The 8042 has three ports:

- An 8-bit output port for system function control and keyboard communication
- An 8-bit input port to read system function status
- A 2-bit test port to read the status of the keyboard Clock and Data lines.

To write to the output port:

1. Write command D1h (next byte is a value byte) to I/O address 64h.
2. Write the desired value for the output port to port address 60h.

To read the 8042 output port value:

1. Write command D0h (transfer the current output port values to the 8042 output buffer) to port address 64h.
2. Read the 8042 output buffer (port address 60h).

Figure 2-57 shows the bit values for the output port of the 8042.

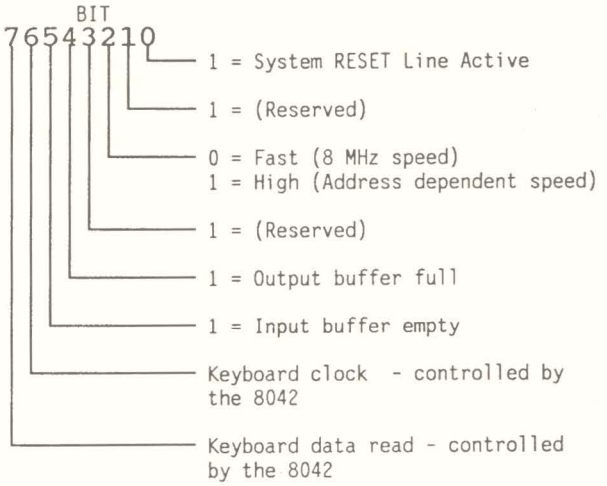


Figure 2-57. 8042 Output Port - Bit Definition

To read the 8042 input port value:

1. Write command C0h (transfer the current input port values to the 8042 output buffer) to I/O address 64h.
2. Read the 8042 output buffer (port address 60h) with the special read command A5h.

Figure 2-58 shows the format of the byte returned from the 8042 input port.

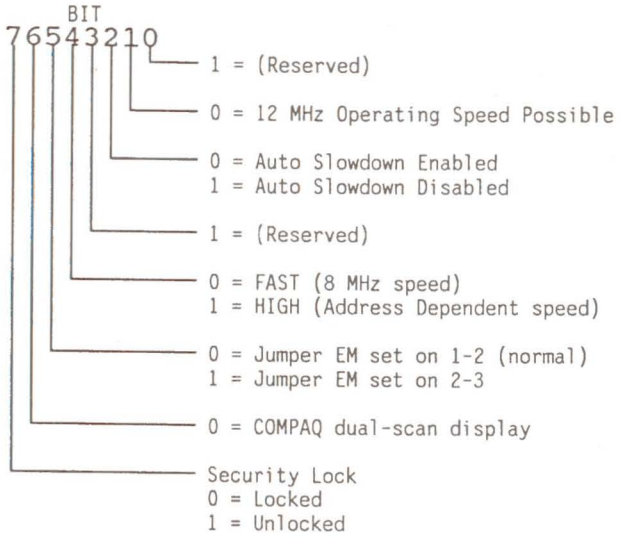


Figure 2-58. 8042 Input Port - Bit Definition

To read the 8042 TEST input port value:

1. Write the command E0h (transfer the current TEST input port values to the 8042 output buffer) to I/O address 64h.
2. Read the 8042 output buffer (port address 60h).

Figure 2-59 shows the format of the byte returned by the 8042 TEST input port.

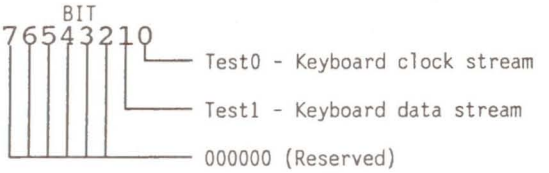


Figure 2-59. 8042 Test Input Port - Bit Definition

Programming the 8042

The 8042 is I/O-mapped at port addresses 60h and 64h.

Prior to writing a command or data to ports 60h or 64h, the 8042 Status register must indicate "Input Buffer Empty". Also, prior to reading data from port 60h, test the 8042 Status register to ensure a "Data in Buffer" condition.

Port 60h, Data I/O Register. Use the 80286's IN instruction to read data from the 8042's output buffer. Data in the Data I/O register is from the keyboard, unless the 8042 has been given a command such as 20h, Read Command byte.

Use the 80286's OUT instruction to send data to the keyboard, unless the 8042 has been given a multibyte command such as 60h, Write Command Byte. To give a multibyte command to the keyboard, write the first command byte to port 64h and the second command byte to 60h.

Port 64h, Command/Status Register. The following pages describe the format for Command/Status register (port 64h) I/O interactions with the 8042.

Use the 80286's IN instruction to read the status of the 8042 and the keyboard (input from port 64h). Use the 80286's OUT instruction to give a command to the 8042 (output to port 64h). Writing to this address automatically sets the COMMAND/DATA flag to 1.

Most commands involve a single write step. However, some commands do require a second step, such as a subsequent 8042 register read or write.

Figure 2-60 shows the 8042 Status register. Figure 2-61 shows the 8042 command byte. Table 2-40 lists the 8042 command codes.

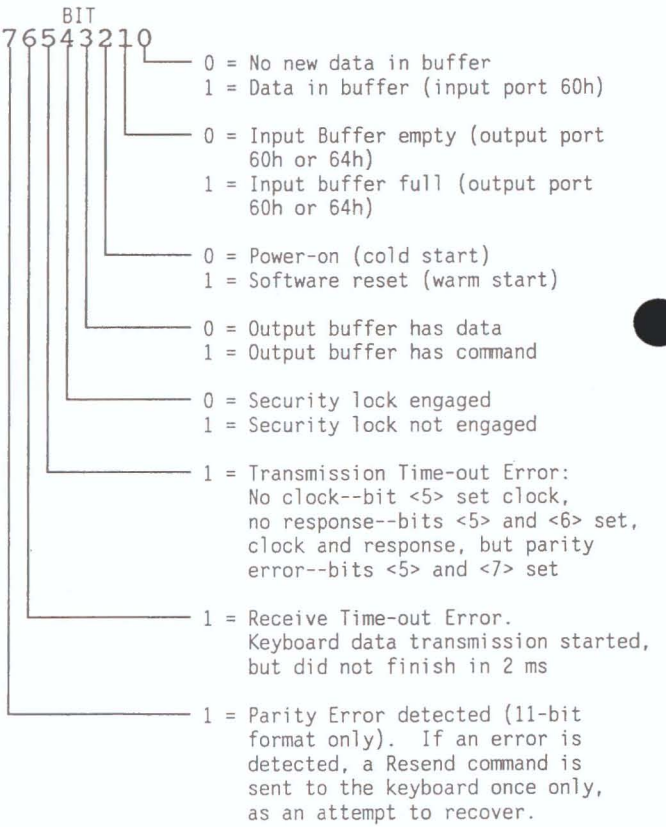


Figure 2-60. 8042 Status Register (Input Port 64h)

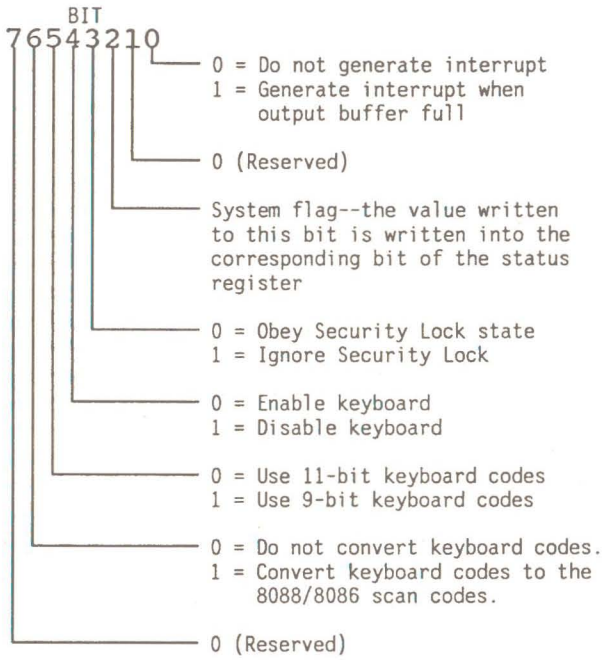


Figure 2-61. 8042 Command Byte (Output Port 64h).

Table 2-40. 8042 Command Codes (Output Port 64)

Code	Function
20h	Put the current command byte on the 8042's output port
60h	Load the next byte put into the 8042's input port as the command byte
A1h	FAST Speed--the 8042 output port selects the 8-MHz speed (SLOWDOWN bit = 0)
A2h	HIGH Speed--the 8042 output port selects an address-dependent speed (SLOWDOWN bit = 1.)
A4h	Toggle--the 8042 changes its speed-control output port bit between the FAST mode speed and the speed defined with the HIGHSP command (A6h).
A5h	Special Read--the 8042 places the real value of port 2 except for bits <4> and <5> which are given a new definition in the output buffer. No output-buffer full is generated. If bit <5> = 0 then a 9-bit keyboard is in use If bit <5> = 1, then an 11-bit keyboard is in use If bit <4> = 0, the interrupt is disabled If bit <4> = 1, when the output buffer full interrupt is enabled
A6h	HIGHSP--the 8042 interprets the next byte written to port 60h as the maximum speed for the system when the Toggle command (A4h) is used. Value Highest Speed 00h FAST (8 MHz) 01h HIGH (address-dependent speed) Note: Only the least-significant bit is used. The other bits should be set to 0.

(Continued)

Table 2-40. (Continued)

Code	Function
AAh	Initialization--the 8042 initializes ports 1 and 2 to their setup value, sets HIGHSP (CPU speed) to the value set by the jumper, disables the keyboard and clears the buffer pointers. It then places 55h in the output buffer.
ABh	Interface Test--directs the 8042 to test the data and clock lines of the keyboard interface. The output buffer (input port 60h) receives the test results, according to: 00h - No error detected 01h - The keyboard Clock line is stuck low 02h - The keyboard Clock line is stuck high 03h - The keyboard Data line is stuck low 04h - The keyboard Data line is stuck high 05h - COMPAQ diagnostic feature Note: The keyboard Data line test does not check for line stuck low for 9-bit keyboards.
ACh	Diagnostic Dump--Reserved for diagnostic purposes.
ADh	Disable Keyboard--sets bit <4> of the 8042's command byte, which disables the keyboard interface. Data are not sent or received until the keyboard is enabled.
AEh	Enable Keyboard--resets bit <4> of the 8042's command byte, which enables the keyboard interface.
C0h	Read Input Port--directs the 8042 to transfer the status of the input port and place it in the output buffer (input port 60h). Use this command only when the output buffer is empty.
D0h	Read Output Port--directs the 8042 to transfer the current byte in the output port to the output buffer (input port 60h). The values for the SPEEDUP and SLOWDOWN bits (D6 and D7) will not be accurate. Use the Special Read command (A5h) to read the correct values. Use the Read Output Port command only when the output buffer is empty.

(Continued)

Table 2-40. (Continued)

Code	Function
D1h	Write Output Port--place the next byte written to the 8042 data register (output port 60h) on the 8042's output port. The system speed bits are not set by this command--use commands A1h to A6h for speed functions.
	CAUTION Setting bit <0> of the 8042's Output Port 0 puts the system in a reset state until the power is turned off.
E0h	Read Test0 and Test1 Inputs--directs the 8042 to put the current state of Test0 and Test1 into the output buffer (output port 60h). Test0 is bit <0> and Test1 is bit<1>.
F0h-FFh	Pulse Output Port--the 8042's output port, bits <3..0>, can be pulsed (strobed low) for approximately 2 us. Bits <3..0> of this command byte each represent one bit, or signal of the output port to be pulsed. Note: Bit <0> of the 8042's Output Port 0 is connected to the system reset. Pulsing bit <0> resets the system.

System Scan Codes

Table 2-41 shows the codes sent by the keyboard to the 8042 for each key, and the final code sent to the system by the 8042.

Table 2-41. Keyboard Scan Codes

U.S. Character	11-bit Keyboard Scan Code	System Scan Code	9-Bit Keyboard Scan Code
	00h	FFh (Note 1)	
ESC	76h	01h	01h
1,!	16h	02h	02h
2,@	1Eh	03h	03h
3,#	26h	04h	04h
4,$	25h	05h	05h
5,%	2Eh	06h	06h
6,^	36h	07h	07h
7,&	3Dh	08h	08h
8,*	3Eh	09h	09h
9,(	46h	0Ah	0Ah
0,)	45h	0Bh	0Bh
-,_	4Eh	0Ch	0Ch
=,+	55h	0Dh	0Dh
<--	66h	0Eh	0Eh

(Continued)

Table 2-41. (Continued)

U.S. Character	11-bit Keyboard Scan Code	System Scan Code	9-Bit Keyboard Scan Code
Tab	0Dh	0Fh	0Fh
Q	15h	10h	10h
W	1Dh	11h	11h
E	24h	12h	12h
R	2Dh	13h	13h
T	2Ch	14h	14h
Y	35h	15h	15h
U	3Ch	16h	16h
I	43h	17h	17h
O	44h	18h	18h
P	4Dh	19h	19h
[,{	54h	1Ah	1Ah
],}	5Bh	1Bh	1Bh
RET	5Ah	1Ch	1Ch
Ctrl	14h	1Dh	1Dh
A	1Ch	1Eh	1Eh
S	1Bh	1Fh	1Fh
D	23h	20h	20h
F	2Bh	21h	21h
G	34h	22h	22h

(Continued)

Table 2-41. (Continued)

U.S. Character	11-bit Keyboard Scan Code	System Scan Code	9-Bit Keyboard Scan Code
H	33h	23h	23h
J	3Bh	24h	24h
K	42h	25h	25h
L	4Bh	26h	26h
;,:	4Ch	27h	27h
','	52h	28h	28h
`,~	0Eh	29h	29h
Lshift	12h	2Ah	2Ah
\,|	5Dh	2Bh	2Bh
Z	1Ah	2Ch	2Ch
X	22h	2Dh	2Dh
C	21h	2Eh	2Eh
V	2Ah	2Fh	2Fh
B	32h	30h	30h
N	31h	31h	31h
M	3Ah	32h	32h
,,<	41h	33h	33h
.,>	49h	34h	34h
/,?	4Ah	35h	35h
Rshift	59h	36h	36h
*,PrtSc	7Ch	37h	37h

(Continued)

Table 2-41. (Continued)

U.S. Character	11-bit Keyboard Scan Code	System Scan Code	9-Bit Keyboard Scan Code
Alt	11h	38h	38h
Space	29h	39h	39h
Caps Lock	58h	3Ah	3Ah
F1	05h	3Bh	3Bh
F2	06h	3Ch	3Ch
F3	04h	3Dh	3Dh
F4	0Ch	3Eh	3Eh
F5	03h	3Fh	3Fh
F6	0Bh	40h	40h
F7	02h,83h (Note 2)	41h	41h
F8	0Ah	42h	42h
F9	01h	43h	43h
F10	09h	44h	44h
Num Lock	77h	45h	45h
Scroll Lock	7Eh	46h	46h
Home,7	6Ch	47h	47h
Up,8	75h	48h	48h
PgUp,9	7Dh	49h	49h

(Continued)

Table 2-41. (Continued)

U.S. Character	11-bit Keyboard Scan Code	System Scan Code	9-Bit Keyboard Scan Code
-	7Bh	4Ah	4Ah
Left,4	6Bh	4Bh	4Bh
5	73h	4Ch	4Ch
Right,6	74h	4Dh	4Dh
+	79h	4Eh	4Eh
End,1	69h	4Fh	4Fh
Down,2	72h	50h	50h
PgDn,3	7Ah	51h	51h
Ins,0	70h	52h	52h
Del,.	71h	53h	53h
Sys Req	7Fh,84h (Note 2)	54h	

(Continued)

Table 2-41. (Continued)

US Character	11-bit Keyboard Scan Code	System Scan Code	9-Bit Keyboard Scan Code
R (Note 3)	60h	55h	
R (Note 3)	61h	56h	
F11 (Note 4)	78h	57h	
F12 (Note 4)	07h	58h	
R (Note 3)		59h through 7Fh	

Notes: 1. When the 8042 cannot read data from the keyboard, the 8042 sends FFh to the system, and sets the parity error bit of the Status register.

2. The second value is generated when the 8042 translates a 9-bit code to an 11-bit code.

3. R = Reserved

4. The F11 and F12 keys (System Scan Codes 57H and 58h respectively) are only available on the COMPAQ Enhanced Keyboard.

8042/Keyboard Communications Time Restraints

If a code transmission from the keyboard exceeds 2 ms, a time-out error results and the 8042 sends FFh to the system. No retries are attempted from a time-out error.

A keyboard Clock signal strobes the 8042 during a data transmission to cycle data bits from the 8042 to the keyboard.

If the keyboard clock does not begin strobing within 15 ms after a byte is ready to transmit, or if the byte is not completely transmitted within 2 ms, the 8042 sends FEh to the system and sets the transmit time-out error bit in the Status register.

The keyboard must respond to all transmissions from the 8042 within 25 ms, or the parity and time-out error bits are set in the Status register of the 8042 and FEh is sent to the system. No retries are attempted by the 8042 after any data transmission error.

Security Key Lock

The security key lock is connected to the P17 line of the 8042 keyboard processor. When the security lock is unlocked, the keyboard is disabled. This feature allows a program to continue without accidental interference.

Interval Timer

The purpose of a programmable interval timer is to generate pulses at software-controllable intervals.

An Intel 8254 Programmable Interval Counter on the system boards provide three frequencies, or timed pulses, for the system. The three counters count down a 16-bit value at a rate of 1.193 million counts-per-second and give an output pulse on the OUT pins. Table 2-42 lists the interval timer functions.

Two channels (interrupt and refresh) are on at all times; only the speaker tone can be disabled and enabled.

Table 2-42. Interval Timer Functions

Function	System Timer
Counter 0:	
Gate	Always On
Clock In	1.193 MHz
Clock Out	8259A IRQ0
Counter 1:	
Gate	Always On
Clock In	1.193 MHz
Clock Out	Request Refresh
Counter 2:	
Gate	Programmable
Clock In	1.193 MHz
Clock Out	Speaker Input

Interval Timer Architecture

The interval timer contains three identical counters. Figure 2-62 shows the architecture of the interval timer. CRm and CRl contain the most- and least-significant bytes of the 16-bit initial count value. These registers are cleared when they are both transferred into CE.

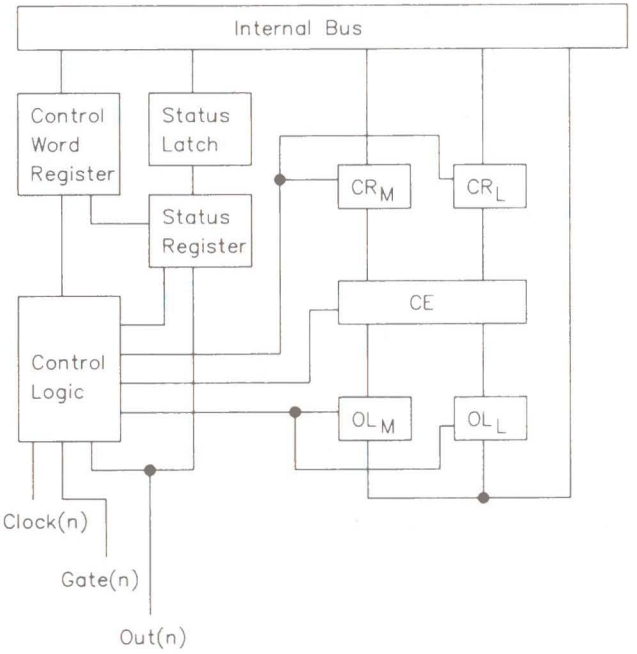


Figure 2-62. Counter Architecture

CE is the actual "Counting Element" latch that contains the value being counted down.

OLm and OLl contain the most- and least-significant bytes of the CE value, unless a latch command is given. In this case, the OLm and OLl registers hold the count until read.

Programming the Interval Timer

The timer is an I/O-mapped device. Table 2-43 lists the ports used. Several commands are available:

- The Control Word specifies:
  - which counter to read or write
  - the operating mode
  - the count format
- The Counter Latch command latches the current count so that it can be read by the system. The count-down process continues.
- The Read Back command reads the count value, programmed mode, the current state of the OUT pins, and the state of the null count flag of the selected counter.

Table 2-43. Interval Timer Port Assignments

Port	Function
40h	Read or Write Count for Counter 0 (System Clock)
41h	Read or Write Count for Counter 1 (Refresh Request)
42h	Read or Write Count for Counter 2 (Speaker Tone)
43h	Input for Control Word, Counter Latch, or Read Back commands (Command Mode Register)

Interval Timer Operating Modes and Initial Values

Six operating modes are available and are listed in Table 2-44.

Table 2-44. Interval Timer Operating Modes

Mode	Function
0	Out signal on end-of-count (=0)
1	Hardware retriggerable one-shot
2	Rate generator (divide-by-n counter)
3	Square-wave output
4	Software-triggered strobe
5	Hardware-triggered strobe

The three counters are initialized with the values given in Table 2-45.

Table 2-45. Interval Timer Initial Values

Counter	Mode	Control Word	Count	Frequency
0	3	36h	65535	18.207 Hz
1	2	54h (See Note)	19	62.799 KHz
2	3	B6h	1336	893.10 Hz

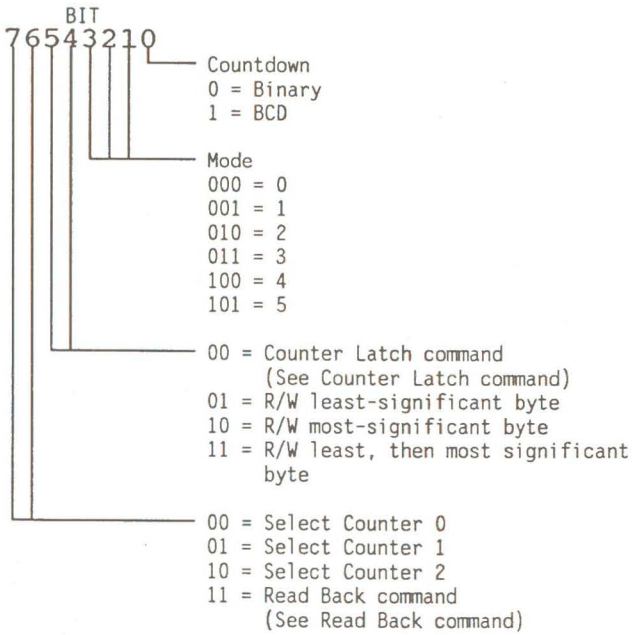
Note: Only the least-significant byte of the divisor is loaded.

Programming the interval timer is a simple process:

1. Write a control word.
2. Write an initial count for each counter.
3. Load the least- and most-significant bytes of the 16-bit counter in two steps (writes).

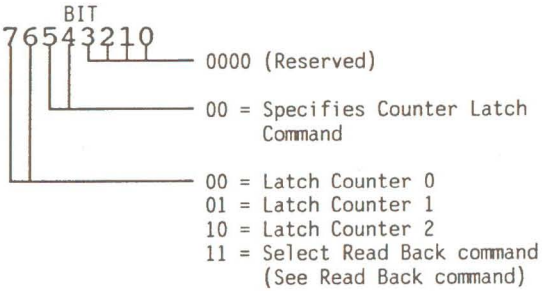
Interval Timer Control Word Format

The Control Word specifies the counter, whether it is to be written to or read from, the operating mode, and whether it counts down in a 16-bit or binary-coded decimal (BCD) format.



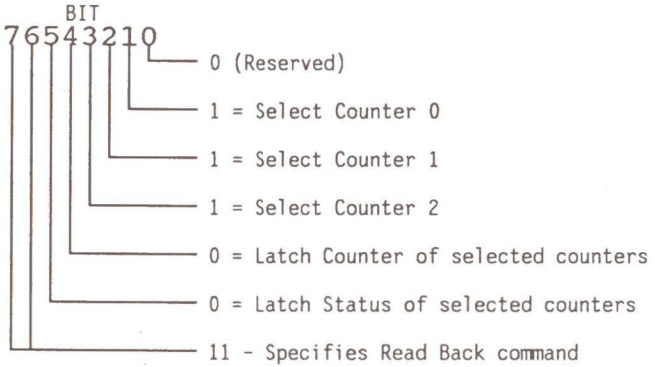
Interval Timer Counter-latch Command

The Counter Latch command latches the count at the time the command is received. The count is held in the OL registers until read.

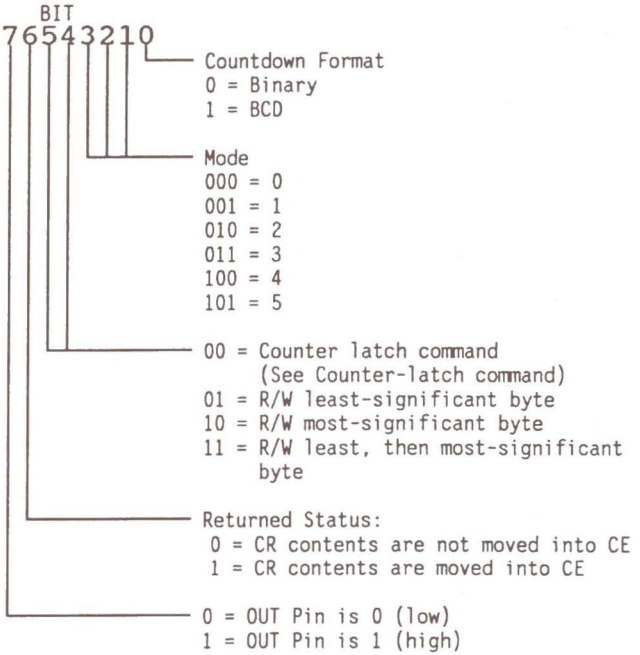


Interval Timer Read Back Command

The Read Back command causes the count or status of the counters to be latched in the OL registers until read. A single read-back can latch the count or status of all three counters.



The status byte latched into OL has the following format:



Interrupt Priority Encoders

The 80286 processor has two signals for interrupts, labelled NMI (nonmaskable interrupt) and INTR (maskable interrupts). A maskable interrupt is an interrupt that can be enabled or disabled by the processor STI/CLI instructions. A nonmaskable interrupt is not masked off by the CLI instruction but can be disabled under software control by the system board logic.

NMI Interrupts

NMI interrupts are caused by parity errors on the system board, memory boards, or any expansion boards that pull the IOCHK- line low.

System software can also generate a software interrupt to the NMI routine. When the IOCHK- line is pulled low, it sets the IOCHK- latch, which holds the error condition until software can examine it.

The source of the NMI can be determined by examining input port 61h, bit <6>. If this bit is set, the interrupt came from the hardware IOCHK- line. To clear the hardware IOCHK- latch, pulse bit <3> of port 61h high.

The mask register for the NMI interrupt is at I/O-address 70h. The format for this byte is 10000000, that is, only the most significant bit is decoded. Write an 80h to port 70h to mask the NMI signal. This port is shared with the real-time clock and configuration memory device (the lower 6 bits). Do not modify the contents of this register without considering the effects on the state of the other bits.

INTR Interrupts

All INTR-type interrupts to the CPU are channelled through the interrupt controllers (8259A). These devices generate interrupts on the 80286's interrupt line, which can be masked in the 80286 by software.

The interrupt controllers are 8-input devices that can accept interrupt signals from several devices, then prioritize them and interrupt the processor. The processor then automatically reads the interrupt controller to determine the source of the highest-priority interrupt and calls the appropriate interrupt routine.

Two interrupt controllers (a master and a slave) are used so that more than eight levels of interrupt are possible. The slave (Interrupt Controller 2) interrupts the master (Interrupt Controller 1)

to show an interrupt. When Interrupt Controller 1 is properly programmed (in the special fully nested mode) Interrupt Controller 2 sends the correct interrupt vector to the CPU for the source of the interrupt. Figure 2-63 shows a diagram of the interrupt controller circuit.

All interrupts can be masked off, using the CLI instruction of the 80286. The base I/O address for Interrupt Controller 1 is 20h; for Interrupt Controller 2 it is A0h. Table 2-46 lists the initial interrupt controller values.

Table 2-46. Initial Interrupt Controller Values

Port	Value	Description of Contents
20h	11h	Cntlr 1, ICW1
21h	08h	Cntlr 1, ICW2 vector address for 000020h
21h	04h	Cntlr 1, ICW3 indicates slave connection
21h	01h	Cntlr 1, ICW4 8086 mode
A0h	11h	Cntlr 2, ICW1
A1h	70h	Cntlr 2, ICW2 vector address for 0001C0h
A1h	02h	Cntlr 2, ICW3 indicates slave ID
A1h	01h	Cntlr 2, ICW4 8086 mode
A21h	B8h	Cntlr 1, Interrupt mask (may vary with option)
A1h	9Dh	Cntlr 2, Interrupt mask (may vary with option)

Table 2-47 lists the 16 possible sources for an interrupt and their priorities. The highest-priority interrupt is processed first.

Table 2-47. Interrupts And Their Priorities

Priority	Label	Controller	Typical Interrupt Source
1	NMI	(Note)	Parity Error Detected
2	IRQ0	1	Interval Timer Output 0
3	IRQ1	1	Keyboard
	IRQ2	1	Interrupt from Controller 2
4	IRQ8	2	Real-Time Clock
5	IRQ9	2	Expansion Bus Pin B04
6	IRQ10	2	Expansion Bus Pin D03
7	IRQ11	2	Expansion Bus Pin D04
8	IRQ12	2	Expansion Bus Pin D05
9	IRQ13	2	Numeric Coprocessor
10	IRQ14	2	Fixed Disk Drive Controller --Expansion Bus Pin D07
11	IRQ15	2	Expansion Bus Pin D06
12	IRQ3	1	Serial Port 2 --Expansion Bus Pin B25
13	IRQ4	1	Serial Port 1 --Expansion Bus Pin B24
14	IRQ5	1	Parallel Port 2 --Expansion Bus Pin B23
15	IRQ6	1	Diskette Drive Controller --Expansion Bus Pin B22
16	IRQ7	1	Parallel Port 1 --Expansion Bus Pin B21

Note: The NMI signal is controlled through the I/O port 70h, bit <7>.

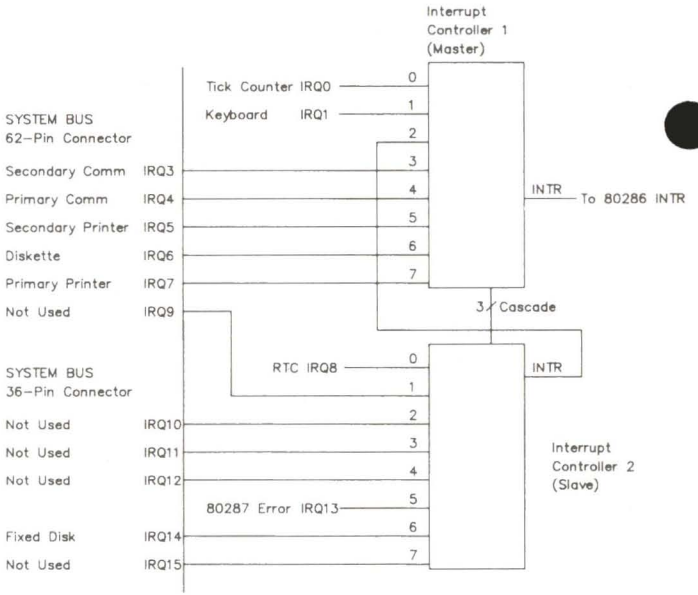


Figure 2-63. Interrupt Controller Circuit Diagram

2.15 EXPANSION BUS

The system board uses expansion slots to support additional circuit boards.

Expansion slots either have two connectors (62-pin and 36-pin) or one connector (62-pin). Slots with both connectors support a 16-bit data bus and the high-order address lines, LA<23..17> as well as additional interrupt and DMA lines. Slots with only one connector support only an 8-bit data bus with address lines SA<19..0>.

This section presents the expansion bus and the system timing requirements and includes:

- Detailed explanations of the expansion bus signals
- Major functions supplied to the expansion bus, such as:
  - Address Handling
  - Data Handling
  - Non-CPU Operations
  - DMA Operations
  - Dynamic RAM Refresh
  - Other Bus Master Operations
- Timing Considerations

Address Handling

When the CPU begins a bus cycle, it places an address on the address bus. This address may be placed on the bus even while the previous cycle is still in progress. Since most devices expect to see a valid address for the duration of a bus cycle, the system board latches the address onto the system bus.

System bus lines that contain the latched address are SA<19..0>. These latches are of the fall-through type so that when the address latch enable signal (ALE) goes active, the address appears at the output. When ALE goes inactive, the addresses will stay on the outputs until the next bus cycle begins.

Some high speed devices overlap some operations (such as address decoding). To allow this, the system bus provides a set of address lines (LA<23..17>) that are not latched but which provide a greater setup time to do decoding. When the address changes, expansion bus devices may decode the high-order address lines and then latch them using BALE. This allows expansion bus devices to take advantage of addresses for the next bus cycle that may be placed on the bus before the current bus cycle is complete.

When other devices (such as DMA or other bus masters) take control of the system bus, the BALE line is held active for the entire duration of the operation. As a result, expansion bus devices cannot use BALE to latch the high-order address lines. Therefore, LA<23..17> should be held stable for the entire duration of each bus cycle.

Data Handling

Data handling for these products is accomplished with two data buses. The first is the 8-bit bus that is compatible with previous products. It is provided by the SD<7..0> lines. External devices and memory that are limited to 8-bit transfers use this bus and the control lines SMRDC-, SMWTC-, IORC-, and IOWC- to enable or latch data on the bus.

Devices that can transfer data 16 bits at a time must also use the SD<15..8> lines for data transfer. The lines SBHE- and SA0 are used to determine which byte(s) are desired. These devices tell the system board that they are 16-bit devices by setting the M16- or IO16- (as appropriate) when they are addressed. Table 2-48 lists the signal relationships.

During 12-MHz local memory cycles, the MRDC-, MWTC-, SMRDC-, SMWTC-, IROC-, IOWC-, and SBHE- strobes are inhibited on the expansion bus. This allows maximum compatibility with the standard 8-MHz expansion bus.

Table 2-48. M16-, IO16-, SA0, and SBHE- Signal Relationship

M16- or IO16-	SA0	SBHE-	Cycle Type
High	High	----	Odd byte transfer on lines SD<7..0>
High	Low	----	Even-byte transfer on lines SD<7..0>
Low	High	High	Reserved
Low	High	Low	Odd-byte transfer on lines SD<15..8>
Low	Low	High	Even-byte transfer on lines SD<7..0>
Low	Low	Low	Even-word transfer on lines SD<15..0>

Non-CPU Operations

The system board supports several operations that are not related to the processor chip itself. They are refresh, traditional direct memory access, and expansion bus master access. Refresh is provided to prevent loss of data in dynamic RAMs (DRAMs). The other operations are used by expansion bus devices that require access to memory or I/O without processor intervention.

The system board prioritizes the requests for each type of service according to the following rules:

- If the CPU is the bus master, it completes the current processor cycle. (This includes word operations to 8-bit memory, which execute as two single-byte operations).
- If the CPU has an instruction LOCKed, it will complete the instruction.
- There is an automatic LOCK between an interrupt acknowledge and the first bus write in the acknowledge sequence.
- In the 80286 protected-virtual mode, segment-description operations are automatically LOCKed (six words are loaded at one time).
- Refresh and other DMA cycles are started on a first-come, first-served basis after the CPU releases the bus.
- If a refresh is in progress when a DMA cycle is requested, the DMA cycle will be run without allowing the CPU to regain control of the bus.
- If a direct memory cycle is in progress when a refresh is requested, the refresh cycle will be run without allowing the CPU to regain control of the bus.
- The DMA controller will hold the bus until all outstanding DMA requests are handled.
- If a DMA channel is programmed for demand or block transfer modes, the DMA controller will keep the bus for the entire time to complete the programmed operation.
- Wait states or 8-bit memory anywhere in the system can delay the time required to acknowledge a DMA request.

Because of the above conditions, peripheral designers must assume that the latency on any DMA request can be as high as 10-12 us in a typical system using only diskette operations. If more than one DMA device is operating at one time, the latency can be even greater. If a program uses a LOCK prefix before string instructions or uses block- or demand-mode DMA, then the latency could reach the millisecond range.

DMA Operations

The DMA controllers in the system operate as a separate subsystem from the main bus controller. They handle requests from the DMA peripherals, arbitrate between them, and then request access to the system address and control lines from the CPU.

There are two types of DMA: byte and word. One of the DMA controllers is connected to handle byte-DMA operations, the other, word-DMA operations. To simplify the arbitration between sources, the request line from the byte controller is connected to a DMA request line (DRQ4) on the word controller. The word DMA controller is programmed for cascade mode on channel 0 (to which DRQ4 is connected) so that it will not actually place an address on the bus when it acknowledges the byte controller's request.

Byte-DMA Operations

The DMA byte cycle begins when a peripheral sets a DRQ<3..0> line active. The DMA controller then arbitrates among any other pending requests and sets the hold request output active. This line (DRQ4) is connected to the word controller as discussed above which does its arbitration. The word controller then sets its hold request line active which is in turn synchronized and arbitrated by the hold arbitration logic discussed above.

When the system responds to the request with an acknowledge, the word DMA controller will respond with a DAK4, which acts as a hold acknowledge to the byte controller. The byte controller will, after synchronizing the acknowledge, place an address on the bus lines.

Logic drives the SBHE- line in the opposite sense of SA0 in order to satisfy 16 bit devices on the bus. When this is complete, the DMA controller drives the lines IORC-, IOWC-, MWTC-, and MRDC- according to the type of cycle being run. If SA0 is high and the addressed memory is 16-bit, logic routes the data between the low half and high half of the data bus. The data is moved from high to low on memory reads, and from low to high on memory writes.

Word-DMA Operations

Word-DMA operations are only possible between word memory (16 bit) and word peripherals. Also, the DMA cannot operate on an odd-address boundary, on either memory or I/O. The system latches the SA0 and SBHE- lines to enable 16-bit devices on the bus.

The DMA-word cycle begins when a peripheral sets a DRQ5-DRQ7 line active. The DMA controllers then arbitrate among any other pending requests and set the hold request output active.

When the system responds to the request, the word DMA controller will, after synchronizing the acknowledge, respond with a DAKx acknowledge to the peripheral. The DMA controller will place the address on the bus and then drive the control lines.

Dynamic RAM Refresh

The dynamic RAM refresh subsystem is designed to do a memory read cycle on each of 512 addresses in the memory space as addressed by SA<8..0>. The other address lines are in an undefined state during the RAM refresh time. The system can also be driven by an external source if another bus master has control.

The system consists of a timer (part of the 8254) that generates the refresh requests every 15.924 us, arbitration logic that arbitrates whether the refresh controller or the DMA subsystem gets control of the bus, a timing generator, and a refresh address counter. The refresh request rate of 62.799 kHz provides 128 refresh cycles in 2.038 ms or 256 cycles in 4.0765 ms or 512 cycles in 8.153 ms.

If an external bus master wishes to take the bus for long periods of time, it must perform refresh or risk losing the contents of dynamic memory. The external bus master can do this by developing its own refresh request timer and internal arbitration.

When it is not otherwise driving the bus, but still has bus control, the bus master can generate a refresh cycle by pulling the REFRESH- line low with an open collector gate. When the MRDC- line goes inactive from the refresh cycle, the REFRESH- line should be released. The external bus master can then take full control.

Other Bus-Master Operations

This system allows other bus masters to take over the system buses and use the I/O peripherals and memory. This is accomplished by the bus master software programming an unused DMA channel for cascade operation. When this is complete, the bus master can request the bus by setting the appropriate DRQx (<7..5>, <3..0>) line active and waiting for a response.

When the system responds with DAKx, the bus master can pull the GRAB- line active (low), disabling the address, data, and control lines. The bus master should then wait one BCLK period before enabling its own buffers with valid address information and wait one more BCLK period before driving the control lines.

When the bus master is finished, it should release the GRAB- and DRQx lines to allow the CPU to continue operations. If the bus master keeps control of the bus for more than 15 us, then it must provide its own refresh timing and request logic to prevent loss of dynamic memory contents.

Bus Driving/Loading Information

The following information is provided to improve the probability that third-party controller boards will work with the standard COMPAQ boards and options.

On bus lines that can be driven by a controller board, the driver should be able to sink a minimum of 20 mA and source 10 mA at 0.5 Vdc and 2.4 Vdc respectively.

On bus lines that are driven in the low direction only (open collector), the driver should be able to sink 20 mA at 0.5 Vdc.

The load on any logic line from a single bus slot should not exceed -2.0 mA in the low state (at 0.5 Vdc) or 0.1 mA in the high state (at 2.7 Vdc).

The logic-high voltage at the expansion bus ranges from 2.0 Vdc to 5.5 Vdc. The logic low voltage at the expansion bus ranges from -1.2 Vdc to 0.8 Vdc.

Bus Timing Information

In the HIGH mode, the system clock toggles between two frequencies (12 MHz or 8 MHz) according to address, in which case the new speed will occur during the BALE time

During these changes, the bus timings for the affected cycles will be somewhere between the actual 12 MHz and 8 MHz timings. Table 2-49 lists the important timing parameters for the expansion slots. This information assumes that the system clock is at a constant speed of 8 MHz.

NOTE: The expansion bus timing information is provided to aid in a general understanding of the system and is subject to change.

Table 2-49. Expansion Slot Timing Parameters

Address access time from SA<19..0> address lines, 16 bit bus read cycle.	
Access time 8 MHz	228 ns
Address access time from SA<19..1> address lines, 8 bit bus read cycle.	
Access time 8 MHz	603 ns
Address access time from SA0 address line, 8 bit bus read cycle.	
Access time 8 MHz	589 ns
Access time from BALE active, 16 bit bus read cycle.	
Access time 8 MHz	232 ns
MRDC- Access time, 16-bit bus read cycle.	
Access time 8 MHz	190 ns
IORC- access time, 16-bit bus read cycle.	
Access time 8 MHz	127 ns
MRDC-, IORC-, access time, 8-bit bus read cycle.	
Access time 8 MHz	502 ns
SMRDC- access time, 8-bit bus read cycle.	
Access time 8 MHz	484 ns
CPU read data hold from MRDC-, IROC-, inactive, 8-bit bus cycle.	
Hold 8 MHz	1 ns

(Continued)

Table 2-49. (Continued)

LAx address valid to 16-bit memory command setup.	
Setup 8 MHz	106 ns
16-bit bus memory cycle M16- low delay from LAx address valid.	
Maximum allowed delay 8 MHz	108 ns
BALE valid to 16-bit memory command setup.	
Setup 8 MHz	20 ns
BALE valid to M16- setup.	
Setup 8 MHz	7 ns
SA<19..0> address valid to 16-bit memory command setup.	
Setup 8 MHz	22 ns
SA<19..0> address valid to I/O, 8-bit command setup.	
Setup 8 MHz	84 ns
SA0 address hold from command.	
Hold 8 MHz	96 ns
SA<19..1> address hold from command.	
Hold 8 MHz	110 ns
CPU write data setup to MWTC- active, 16-bit bus memory cycle.	
Setup 8 MHz	-5 ns

(Continued)

Table 2-49. (Continued)

CPU write data setup to IOWC- (16/8-bit), MWTC- (8-bit), active.	
Setup 8 MHz	58 ns
CPU write data setup to MWTC-, IOWC-, inactive, 16-bit bus cycle.	
Setup 8 MHz	245 ns
CPU write data setup to MWTC-, IOWC-, inactive, 8-bit bus cycle.	
Setup 8 MHz	620 ns
Refresh address setup to MRDC- active.	
Setup 8 MHz	76 ns
Refresh address hold from MRDC- inactive.	
Hold 8 Hz	-5 ns
Refresh wait state BUSRDY low delay from MRDC- active.	
Maximum allowed delay 8 MHz	90 ns
Refresh wait state BUSRDY high setup to BCLK rising.	
Setup 8 MHz	5 ns
CPU memory or I/O command wait state BUSRDY high setup to BCLK rising.	
Setup 8 MHz	51 ns
CPU 16-bit memory command wait state. BUSRDY low delay from command active.	
Maximum allowed delay 8 MHz	75 ns

(Continued)

Table 2-49. (Continued)

CPU 16-bit I/O command wait state. BUSRDY low delay from command active.	
Maximum allowed delay 8 MHz	12 ns
CPU 8-bit command wait state. BUSRDY low delay from command active.	
Maximum allowed delay 8 MHz	387 ns
CPU minimum command active from BUSRDY high after added wait state.	
Command active 8 MHz	135 ns
CPU maximum command active from BUSRDY high after added wait state.	
Command active 8 MHz	300 ns
CPU 16-bit memory command no wait state NOWS- low delay from command active.	
Maximum allowed delay 8 MHz	20 ns
CPU 8-bit memory command no wait state NOWS- low setup to BLCK falling required.	
Setup required 8 MHz	16 ns
DMA memory read, I/O write command additional wait state. BUSRDY low delay from memory read command active.	
Maximum allowed delay 8 MHz	182 ns
DMA I/O read, memory write command additional wait state. BUSRDY low delay from I/O read command active.	
Maximum allowed delay 8 MHz	273 ns

(Continued)

Table 2-49. (Continued)

Required I/O data access time from IORC- for DMA write to RAM.	
DMA I/O read access time 8 MHz	264 ns
DATA valid after IOWC- low during DMA read from RAM.	
DMA data valid from IOWC- low 8 MHz	163 ns
DATA setup to IOWC- high during DMA read from RAM.	
Data setup to IOWC- high 8 MHz	217 ns

2.16 MISCELLANEOUS SYSTEM BOARD INFORMATION

This section contains miscellaneous information that does not relate to any of the other sections, such as:

- Speed control
- Real-Time Clock and Configuration-Memory Battery
- Indicators
- Fuses
- Speaker Interface
- Clock Circuits
- System Board Power Requirements

Speed Control

- FAST - I/O speed = 8 MHz, memory speed = 8 MHz
- HIGH - I/O speed = 8 MHz
  Memory Speed (Expansion Bus) = 8 MHz
  Memory Speed (System Board) = 12 MHz
- AUTO - operates in HIGH, except to switch to 8 MHz during diskette operations

In the FAST mode, all memory addresses or bus cycle types operate at 8 MHz except:

- DMA transfers (4 MHz)

The HIGH mode operates the system board RAM and ROM at a faster (12 MHz) speed. In the HIGH mode, the following memory addresses or bus cycle types continue to operate at 8 MHz:

- Memory with addresses 000000h to 09FFFFh not physically located on the system board.
- Memory with addresses 0A0000h to 0DFFFFh
- Memory with addresses 100000h to FDFFFFh not physically located on the system board.
- All I/O devices, except DMA transfers (4 MHz)
- Any 8-bit memory device

In the HIGH mode, the following memory addresses or bus cycle types operate at 12 MHz:

- RAM in base memory (000000h to 09FFFFh) physically located on the system board.
- RAM in extended memory (100000h to FDFFFFh) physically located on the system board
- ROM (0E0000h to 0FFFFFh and FE0000h to FFFFFFh))

The speed is controlled by system software through the keyboard controller (8042).

The AUTO mode is a subset of the HIGH mode. In the AUTO mode, all cycles operate just as in HIGH mode, except the default system speed automatically switches to 8 MHz during diskette operations.

Switch SW1 position 6 together with the AUTO jumper sets the speed of the CPU when the system is powered up. When the speed switch is OFF and AUTO is disabled, the system boots in the HIGH mode, and the CPU speed can be toggled between HIGH and FAST mode using the multiple key combination of Ctrl, Alt, \.

When the speed switch is OFF and AUTO is enabled, the system will boot in the AUTO mode, and the CPU speed can be toggled between AUTO and FAST mode using the multiple key combination of Ctrl, Alt, \.

When the speed switch is ON, the CPU speed is limited to the FAST mode and use of the multiple key combination Ctrl, Alt, \ will not affect the CPU speed.

The MODE SPE[ED] command overrides the speed switch and AUTO jumper settings in all cases.

Real-Time Clock and Configuration-Memory Battery

Table 2-50 lists the battery voltage range at the battery connector under load condition.

Table 2-50. Battery Connector Pinout

Pin	Function	Battery Voltage Min.	Max.
1	+5 VDC Power	5.0	5.4
2	Keyed		
3	Not Used		
4	Ground	0.0	0.0

The voltage for a new battery must not exceed 6.2 V open circuit. The current drain on the battery varies with the voltage and the clock operating mode, but is between 50 to 90 uA after running SETUP. The maximum current is less than 150 uA.

CAUTION

Only COMPAQ Authorized Dealers should replace the system battery. Extreme caution must be observed to replace the battery with an identical battery type and on the correct connector pins.

Indicators (LEDs)

The system board has a light-emitting diode (LED) that lights when the +5 Vdc power is ON.

Fuses

The system board, 12 MHz version, has no user-replaceable fuses.

Speaker Interface

The speaker interface allows the speaker to be driven from two sources: the 8254-2 interval timer 2, or the processor through port 61h bit 1. In addition, the 8254 interval timer 2 can be enabled and disabled from port 61h bit 0.

To use the 8254 interval timer to generate a tone, program Timer 2 to the desired frequency (the input clock rate is 1.193 MHz), and set port 61h bits 0 and 1 to 1. If the speaker is to be toggled directly by the CPU, port 61h bit 0 should be set to 0 and bit 1 should be toggled.

Clock Circuits

The two crystal oscillators on the system board provide:

- Clock frequencies for the 80286 processor and the entire system
- A clock source for video color-burst signal and general timing

A crystal oscillator provides a 48-MHz frequency that is divided by 2 or 3 (software-selected) by the clock-generator interface to provide a master clock for the 80286.

The clock generator interface then divides both the 48-MHz and the master clock to supply the clocks used by the 80287 and other clocked devices. This interface also controls the reset signal. System reset does not occur until power levels are stable (PWRGOOD signal from power supply becomes active).

A second crystal oscillator on the system board provides a 14.31818-MHz (4 times 3.579545 MHz) clock signal for color-burst timing. This clock signal connects to pin B30 of the board slots for use by the video controller and other boards.

System Board Power Requirements

The system board uses +5 VDC and +12 VDC power and distributes power for other components of the system from the -5 VDC, -12 VDC and auxiliary +12 VDC provided by the power supply.

2.17 GATE ARRAY DEVICES

The system board, 12 MHz version, has three gate array devices:

- Memory and Speed Control (MSC) Gate Array
- Clock and Buffer Control (CBC) Gate Array
- Memory Map (MAP) Gate Array

This section describes the Gate Array Devices and provides a functional overview of each device.

MSC Gate Array

The MSC Gate Array includes the memory decoding and speed change functions.

The speed change function indicates whether the system should run at 12 MHz or 8 MHz when operating in the HIGH mode. The memory decoding functions include the generation of chip select and output enable signals, as well as multiple RAS and CAS lines for memory bank and hi/lo byte selection. In addition, the MSC Gate Array provides the address during REFRESH cycles.

CBC Gate Array

The CBC Gate Array provides buffer and clock control. It includes the clock switching/generation logic, generation of automatic and requested wait-states, shutdown logic, 8/16 bit bus conversion, and bus arbitration.

MAP Gate Array

The MAP Gate Array includes the DMA page register, as well as the circuitry for PORT B, SPEAKER and GATE control, REFRESH DETECT, and NMI control.

2.18 JUMPERS AND SWITCHES

The system board, 12 MHz version, has three switch positions not used for memory selection (Figure 2-64). These switch positions are described in Table 2-51.

Table 2-51. System Board Switch SW1 Settings

SW1 Position	Setting	Description
6	CLOSED	CPU speed limit setting - 8 MHz (FAST)
	OPEN	CPU speed toggle active (HIGH/FAST or AUTO/FAST)
8	CLOSED	COMPAQ Graphics or RGBI Video Controller
	OPEN	non-COMPAQ monochrome/text video controller
7	CLOSED	Reserved

Legend: CLOSED = ON, OPEN = OFF

The AUTO jumper (labeled E5 on the system board) settings enables or disables an additional speed option. When AUTO is enabled, the default system speed automatically switches to 8 MHz during diskette drive operations. This allows time-dependent copy schemes to work properly. Table 2-52 lists the AUTO jumper settings.

Table 2-52. AUTO Jumper (E5) Settings

Setting	Description
1-2	AUTO disabled (CPU toggle: HIGH/FAST)
1-2	AUTO enabled (CPU toggle: AUTO/FAST)

Note: The AUTO jumper has no effect if the speed switch is set to limit the CPU speed to FAST.

2.19 CONNECTORS AND EXPANSION SLOTS

Tables 2-53 and 2-54 list the system board connectors and expansion slots, respectively. Table 2-55 describes the expansion slot signals. Figures 2-64 through 2-74 show the connectors on the system board.

Table 2-53. System Board Connections

Function	COMPAQ DESKPRO 286 (12 MHz Only)
DC power(In)	J117
Drive power(Out)	J111-J112
Fixed disk drive power	J109 or J110 (See Note)
Battery	J118
Keyboard	J116
Monitor power	J113
Security lock	J119
Speaker	J115

Note: J110 is for a fixed disk drive back-up or second fixed disk drive.

Table 2-54. System Board Expansion Slots

Slot	62-Pin	36-Pin	Function
1	J101	J121	Expansion (available)
2	J102	N/A	Expansion (available)
3	J103	J123	Expansion (available)
4	J104	J124	Expansion (available)
5	J105	J125	Expansion (available)
6	J106	J126	Fixed Disk Drive Controller
7	J107	J127	Video Display Controller
8	J108	N/A	Diskette/Tape Controller

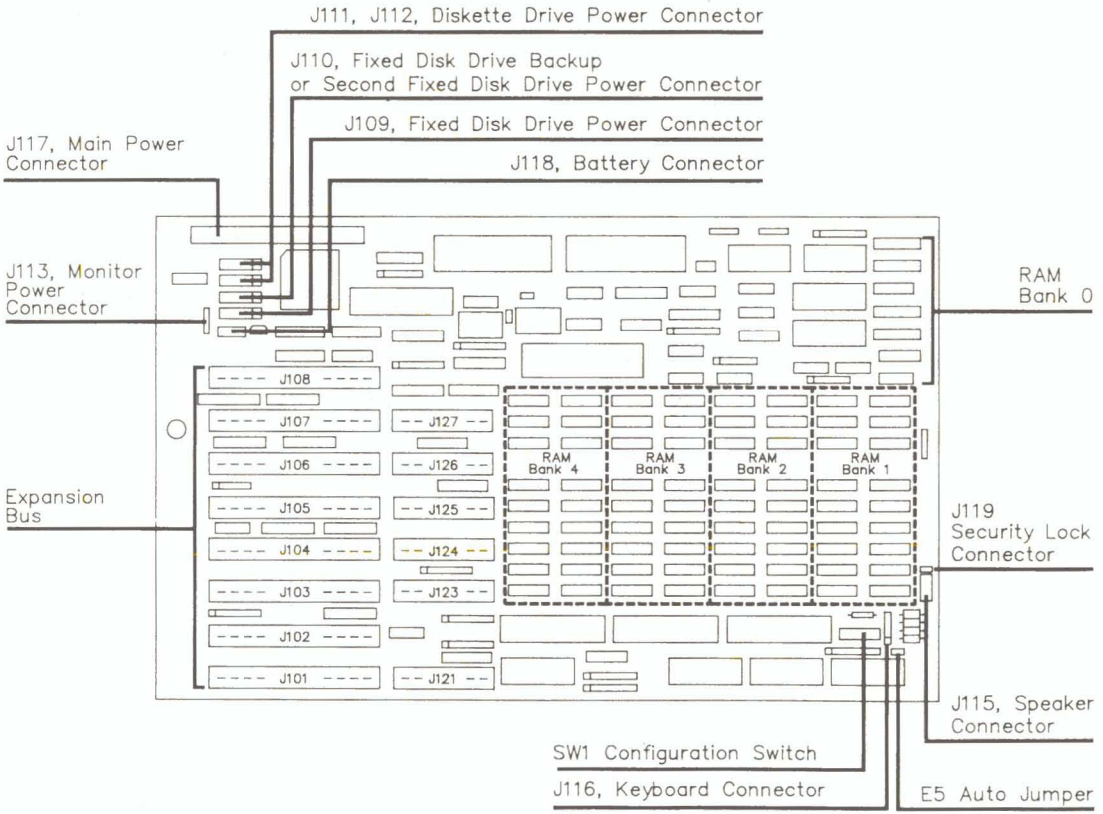


Figure 2-64. System Board Connectors, SW1 Switch, and AUTO Jumper Locations

Table 2-55. Expansion Slot Signals

Signal Name	Slot Pin	Type	Description
AEN	A11	O	This output signal when inactive (low) indicates that the CPU or controller board bus master has control of the bus. When active, the DMA controller has control of the bus. It is often used to disable devices which must not respond during a DMA cycle.
BALE	B28	O	This output signal (when high) indicates that a valid address is present on the LA<23..17> address lines. The LA<23..17> address lines or any decodes developed from them should be latched at the falling edge of BALE. This line is high when a DMA or bus master operation is occurring.
BCLK	B20	O	This output signal is provided to allow synchronization to the main processor clock. Its frequency will be either 8 MHz or 12 MHz.
BUSRDY	A10	I	This input signal is used to lengthen a bus cycle from its standard time if a controller board cannot respond quickly enough. It should be pulled low by an open collector type device as soon as a slow addressed device is selected and held low until the device has responded. Bus cycles are lengthened by an integral number of (BCLK) cycles. This line should not be held low for more than 2.5 us. This line should be driven by an open-collector device capable of sinking 20 mA.
DAK0- DAK1- DAK2- DAK3- DAK5- DAK6- DAK7-	D08 B17 B26 B15 D10 D12 D14	O O O O O O O	These output lines (DMA Acknowledge) indicate that a request for a DMA service from the DMA subsystem has been recognized. The acknowledge is indicated by a LOW on this line. Use this line with the IORC- or IOWC- line to decode the desired DMA device. If used to signal acceptance of a bus-master request, this signal indicates when it is legal to pull GRAB- low.
DRQ0 DRQ1 DRQ2 DRQ3 DRQ5 DRQ6 DRQ7	D09 B18 B06 B16 D11 D13 D15	I I I I I I I	These input lines are used to request a DMA service from the DMA subsystem or to gain control of the system bus from the main CPU (DMA request). The request is made when the line goes from allow to a high and must remain high until the appropriate DAK<7..5>, <3..0> line goes active.

(Continued)

Table 2-55. (Continued)

Signal Name	Slot Pin	Type	Description
GRAB-	D17	I	This input signal is used to indicate that a controller board bus master is controlling the bus. A controller board can pull this line low when the appropriate DAK line is made active, signaling that a master request is granted. The system address, data and control lines will be floated, allowing the controller board to begin controlling them one full BCLK period after GRAB is made active. At least one more full BCLK period should be allowed after putting a valid address on the bus before activating any of the control lines. This line should be driven by an open-collector device capable of sinking 20 mA.
GROUND	B01 B10 B31 D18	-- -- -- --	These lines are connected to the system ac and dc ground. The maximum current allowed on any single contact is 1.5 A.
IOCHK-	A01	I	This input signal is used to signal the CPU about parity or other serious errors on controller boards. This signal should be driven low by an open collector type output capable of sinking 20 mA when an uncorrectable system error occurs.
IORC-	B14	I/O	This output line (I/O read) indicates (when low) when an I/O device is to send data to the data bus. It can be driven by a controller board acting as a bus master.
IOWC-	B13	I/O	This output line (I/O write) indicates (when low) when an I/O device is to accept the data from the data bus. It can be driven by a controller board acting as a bus master.
IO16-	D02	I	This input line (I/O is 16 bits) signals the system that the addressed I/O device is capable of transferring 16 bits of data at once. When this line is made active, during an I/O read or write, the standard one wait state I/O cycle will be run. This line should be driven low by an open-collector device capable of sinking 20 mA.
IRQ3 IRQ4 IRQ5 IRQ6 IRQ7 IRQ9 IRQ10 IRQ11 IRQ12 IRQ14 IRQ15	B25 B24 B23 B22 B21 B04 D03 D04 D05 D07 D06	I I I I I I I I I I I	These input lines are used to interrupt the CPU to request some service. The interrupt is recognized when the line goes from a low to a high and remains there until the appropriate interrupt service routine is executed.

(Continued)

Table 2-55. (Continued)

Signal Name	Slot Pin	Type	Description
LA17 LA18 LA19 LA20 LA21 LA22 LA23	C08 C07 C06 C05 C04 C03 C02	I/O I/O I/O I/O I/O I/O I/O	These output signals (Latchable Address) are used to decode memory which must respond with zero or one wait state. They are only guaranteed to be valid when BALE is high. These can be driven by a controller board acting as a bus master.
MRDC-	C09	I/O	This output line (Memory Read) indicates (when low) when a memory device is to send data to the data bus. This signal is active over the entire address space of the system. It can be driven by a controller board acting as a bus master.
MWTC-	C10	I/O	This output line (Memory Write) indicates (when low) when a memory device is to accept the data from the data bus. This signal is active over the entire address space of the system. It can be driven by a controller board acting as a bus master.
M16-	D01	I	This input line (memory is 16 bits) signals the system that the addressed memory is capable of transferring 16 bits of data at once. When this line is made active, during a memory read or write, the standard one wait state memory cycle will be run. This line should be derived from the LA<23..17> address lines. This line should be driven low by an open collector device capable of sinking 20 mA.
NOWS-	B08	I	This input line (No Wait State) is used to inform the system that standard wait states can be deleted for cycles when this line is made active. The line must be pulled low 45 ns before the falling edge of BCLK in order to be recognized. This line should be driven by an open collector device capable of sinking 20 mA.
OSC	B30	O	This output signal is a clock for use in video color burst and other general timing applications. Its frequency is 14.31818 MHz and duty cycle is approximately 50%.
REFRESH-	B19	I/O	This output signal is used to indicate (when low) a refresh cycle in progress. It should be used to enable the SA<8..0> address lines to the row address inputs of all banks of dynamic memory so that when the MRDC- goes active, the entire system memory is refreshed at one time. It can be driven by a controller board acting as a bus master.
RESDRV	B02	O	This output signal is used to reset the hardware during power-on or power failure.

(Continued)

Table 2-55. (Continued)

Signal Name	Slot Pin	Type	Description
SA0	A31	I/O	These bidirectional signals address memory or I/O devices within the system. They form the low order 20 bits of the 24 bit address bits that the system offers. These lines are enabled onto the bus while BALE is high and are latched when BALE goes from a high to a low state. These can be driven by a controller board acting as a bus master.
SA1	A30	I/O	
SA2	A29	I/O	
SA3	A28	I/O	
SA4	A27	I/O	
SA5	A26	I/O	
SA6	A25	I/O	
SA7	A24	I/O	
SA8	A23	I/O	
SA9	A22	I/O	
SA10	A21	I/O	
SA11	A20	I/O	
SA12	A19	I/O	
SA13	A18	I/O	
SA14	A17	I/O	
SA15	A16	I/O	
SA16	A15	I/O	
SA17	A14	I/O	
SA18	A13	I/O	
SA19	A12	I/O	
SBHE-	C01	I/O	This output signal (System Bus High Enable) indicates (when low) that the high half of the SD data bus should transfer the data on boards which support the full 16-bit data bus. It can be driven by a controller board acting as a bus master.
SD0	A09	I/O	These bidirectional signals are the low 8 bits of the system data bus. They should be used exclusively by all eight bit devices to transfer data. Sixteen-bit devices should use these lines to transfer only the low half of a data word when the address line A0 is low. These can be driven by a controller board acting as a bus master.
SD1	A08	I/O	
SD2	A07	I/O	
SD3	A06	I/O	
SD4	A05	I/O	
SD5	A04	I/O	
SD6	A03	I/O	
SD7	A02	I/O	

(Continued)

Table 2-55. (Continued)

Signal Name	Slot Pin	Type	Description
SD08 SD09 SD10 SD11 SD12 SD13 SD14 SD15	C11 C12 C13 C14 C15 C16 C17 C18	I/O I/O I/O I/O I/O I/O I/O I/O	These bidirectional signals are the high 8 bits of the system data bus. Sixteen bit devices should use these lines to transfer the high half of a data word when the line SBHE- is low. These can be driven by a controller board acting as a bus master.
SMRDC-	B12	O	This output line (Standard Memory Read) is active (low) only when an address from 000000h to 0FFFFFh is decoded. This line is derived from MRDC-.
SMWTC-	B11	O	This output line (Standard Memory Write) is active (low) only when an address from 000000h to 0FFFFFh is decoded. This line is derived from MWTC-.
T/C	B27	O	This output signal (when high) indicates that the Terminal Count of a DMA operation has been reached. It should be decoded with the appropriate DAKx line for proper operation.
+5 Vdc	B03 B29 D16	-- -- --	These lines are connected to the system power supply for 5 volts. In addition to the maximum current available from the supply, the maximum current allowed on any single contact is 1.5 A.
-5 Vdc	B05	--	This line is connected to the system power supply for minus 5 volts. This supply is intended for low-current usage only (500 mA).
-12 Vdc	B07	--	This line is connected to the system power supply for minus 12 volts. This supply is intended for low-current usage only (1.0 A).
+12 Vdc	B09	--	This line is connected to the system power supply for 12 volts. In addition to the maximum current available from the supply, the maximum current allowed on this contact is 1.5 A.

The 36-pin connector conducts the high-order byte of the 16-bit data bus, the memory address lines for bits DAK<7..5>, LA<23..17>, signals, and more. These signals generally relate to 16-bit or high-address memory transfers.

The 62-pin connector conducts the signals needed by adapters that do not need word-length data transfers or access to more than the base 1 MB of memory.

Figure 2-65 shows the 36-pin connector and the signals that it provides.

Signal	Pin	Pin	Signal
M16–	D01	C01	SBHE–
IO16–	D02	C02	LA23
IRQ10	D03	C03	LA22
IRQ11	D04	C04	LA21
IRQ12	D05	C05	LA20
IRQ15	D06	C06	LA19
IRQ14	D07	C07	LA18
DACK0–	D08	C08	LA17
DRQ0	D09	C09	MRDC–
DACK5–	D10	C10	MWTC–
DRQ5	D11	C11	SD8
DACK6–	D12	C12	SD9
DRQ6	D13	C13	SD10
DACK7–	D14	C14	SD11
DRQ7	D15	C15	SD12
+5 V	D16	C16	SD13
GRAB–	D17	C17	SD14
SIGNAL GROUND	D18	C18	SD15

Figure 2-65. Expansion Slot - 36-Pin Connector

Figure 2-66 shows the 62-pin connector and the signals that it provides.

Signal	Pin	Pin	Signal
GROUND	B01	A01	IOCHK–
RESDRV	B02	A02	SD7
+5 Vdc	B03	A03	SD6
IRQ9	B04	A04	SD5
–5 Vdc	B05	A05	SD4
DRQ2	B06	A06	SD3
–12 Vdc	B07	A07	SD2
NOWS–	B08	A08	SD1
+12 Vdc	B09	A09	SD0
GROUND	B10	A10	BUSRDY
SMWTC–	B11	A11	AEN
SMRDC–	B12	A12	SA19
IOWC–	B13	A13	SA18
IORC–	B14	A14	SA17
DAK3–	B15	A15	SA16
DRQ3	B16	A16	SA15
DAK1–	B17	A17	SA14
DRQ1	B18	A18	SA13
REFRESH–	B19	A19	SA12
BCLK	B20	A20	SA11
IRQ7	B21	A21	SA10
IRQ6	B22	A22	SA9
IRQ5	B23	A23	SA8
IRQ4	B24	A24	SA7
IRQ3	B25	A25	SA6
DAK2–	B26	A26	SA5
T/C	B27	A27	SA4
BALE	B28	A28	SA3
+5 Vdc	B29	A29	SA2
OSC	B30	A30	SA1
SIGNAL GROUND	B31	A31	SA0

Figure 2-66. Expansion Slot - 62-Pin Connector

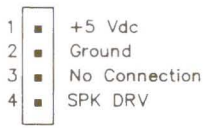


Figure 2-67. J109 and J110, Fixed Disk Drive or Fixed Disk Drive Back up Power Connector

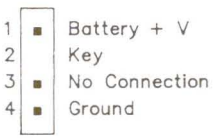


Figure 2-68. J111 and J112, Diskette Drive Power Connectors

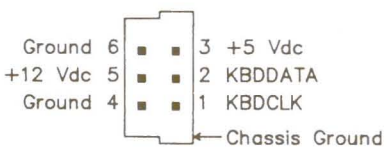


Figure 2-69. J113, Monitor Power Connector

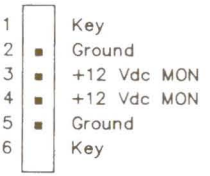


Figure 2-70. J115, Speaker Connector

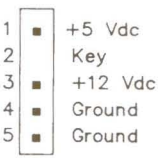
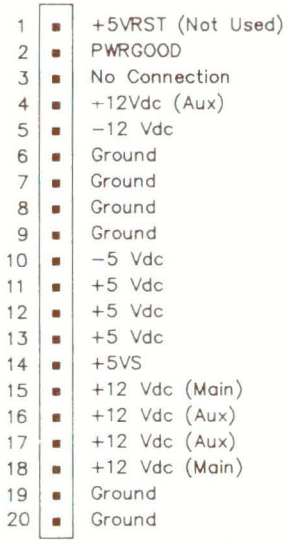


Figure 2-71. J116, Keyboard Connector



Note: The maximum current for a single conductor (pin) must not exceed 5.0 A per line for +5 Vdc or 4.0 A for other lines.

Figure 2-72. J117, Main Power Connector

Figure 2-73. J118, Battery Connector

Figure 2-74. J119, Security Lock Connector

2.20 COMPONENT LAYOUTS AND SCHEMATICS

Figure 2-75 shows the component layout for the COMPAQ DESKPRO 286 system board, 12 MHz version. Figure 2-76 shows the schematics for this system board. Compaq Computer Corporation does not guarantee the accuracy of the component layout or the schematics.

They are provided to aid in a general understanding of the system operation.

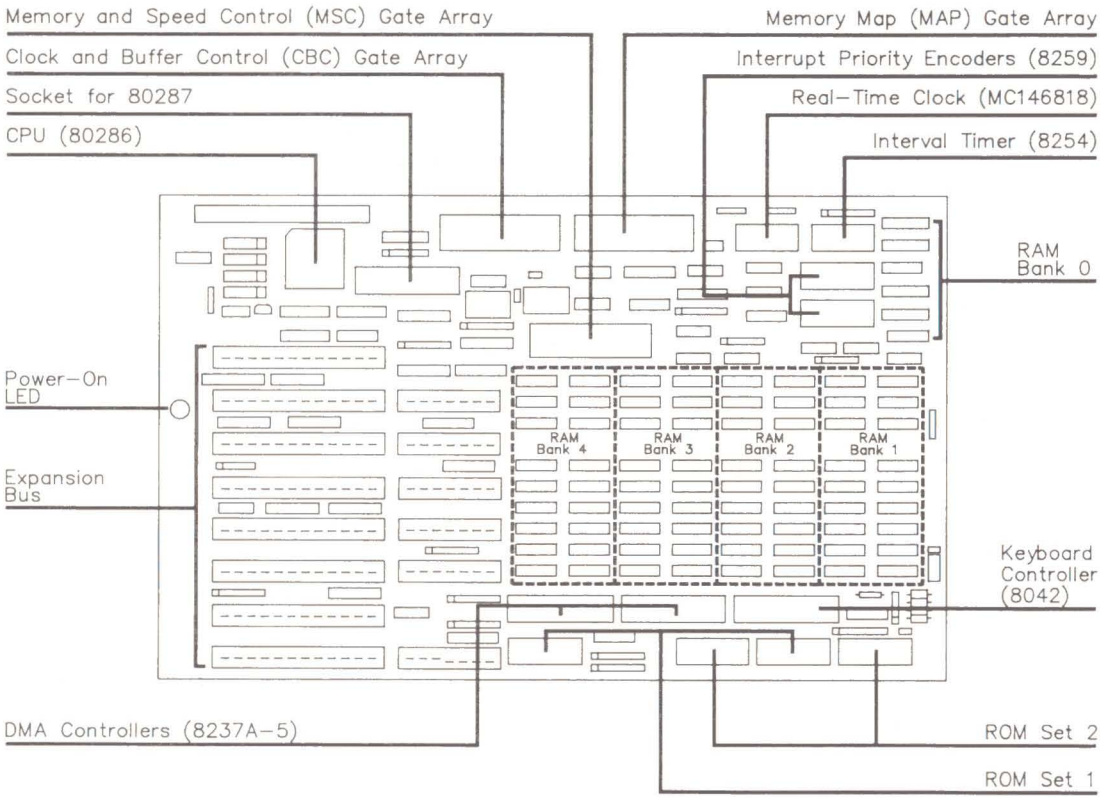


Figure 2-75. The 12 MHz Version COMPAQ DESKPRO 286 System Board Component Layout

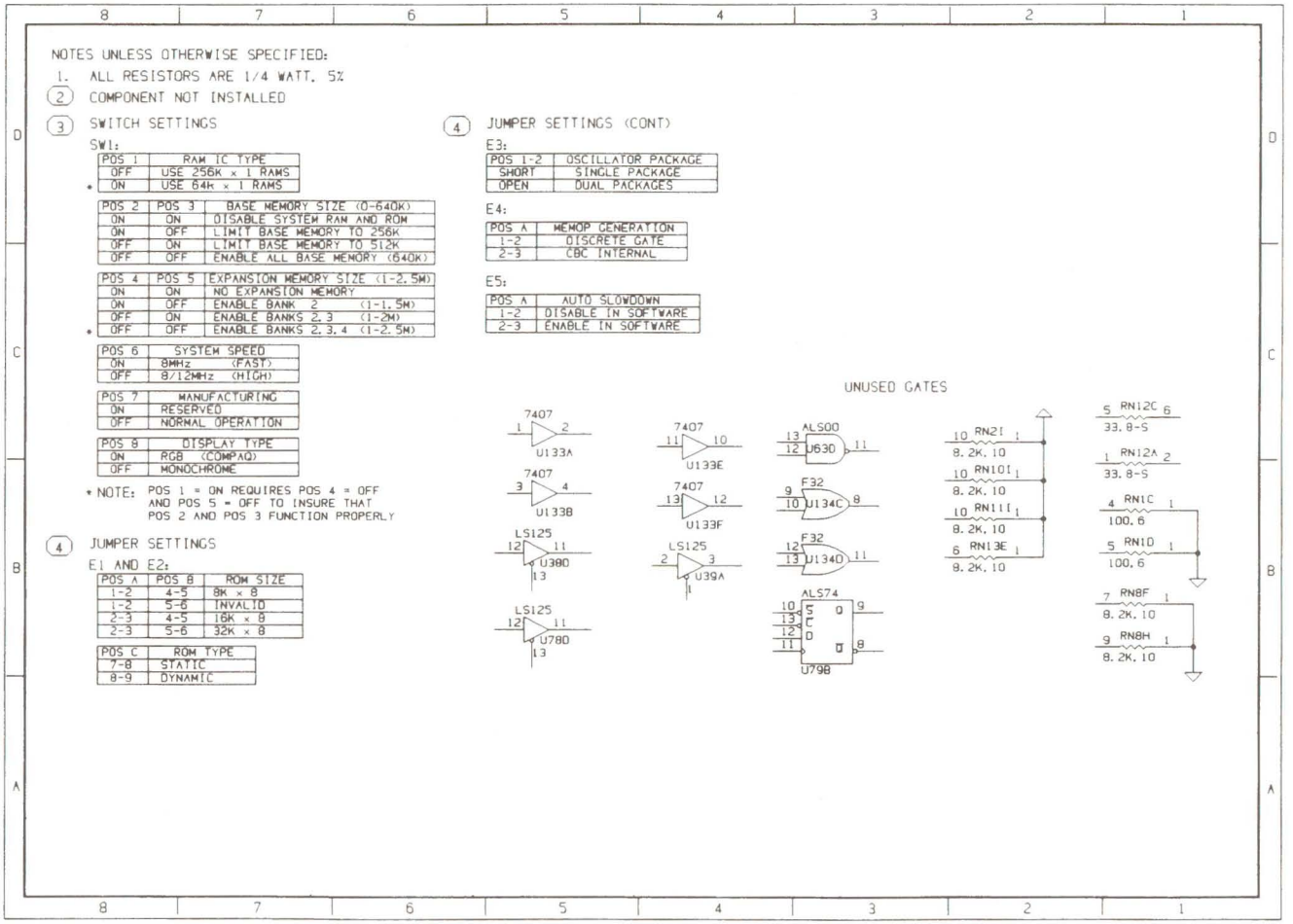


Figure 2-76. The 12 MHz COMPAQ DESKPRO 286 System Board Schematics (Page 1 of 19)

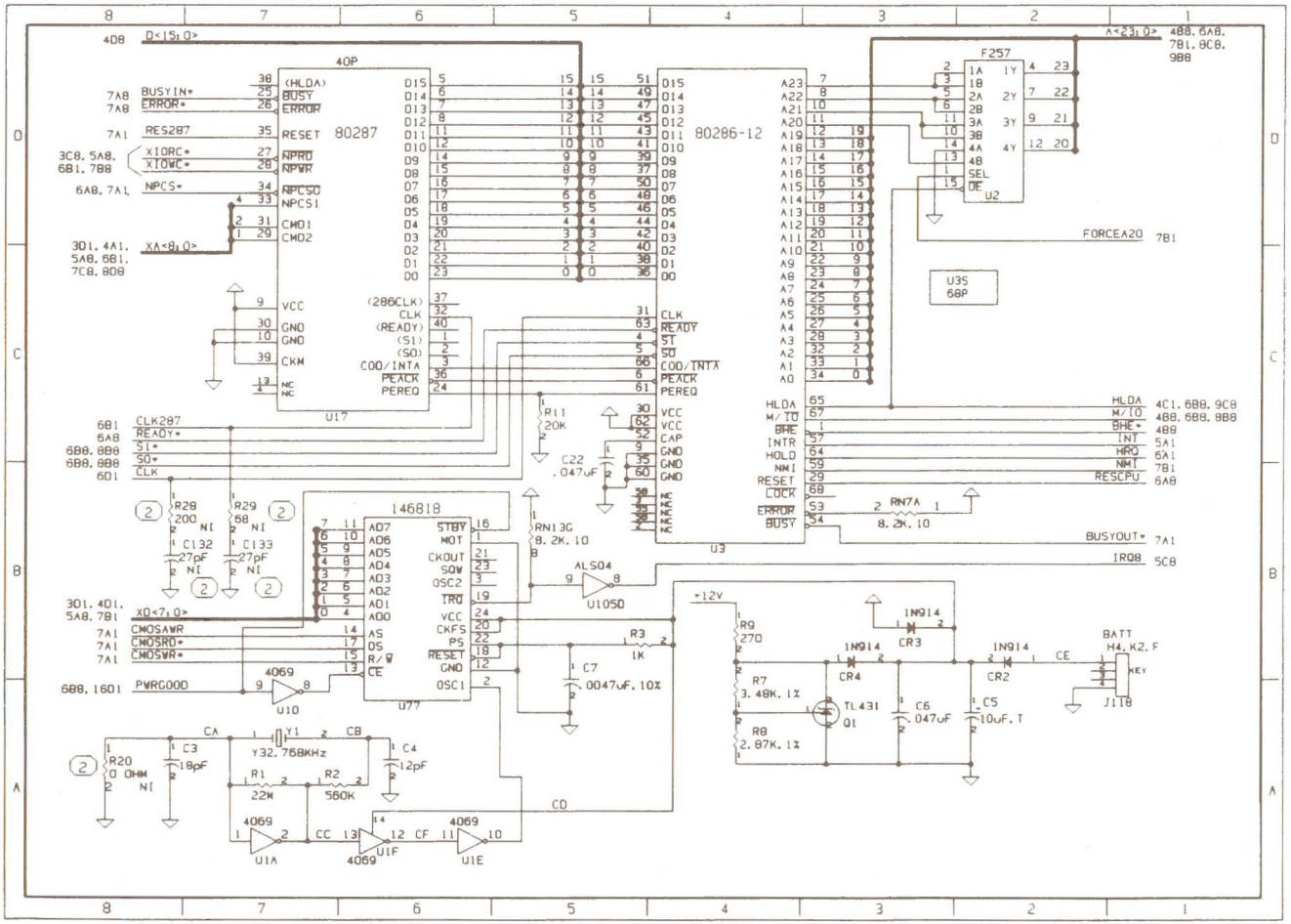


Figure 2-76. The 12 MHz DESKPRO 286 System Board Schematics (Page 2 of 19)

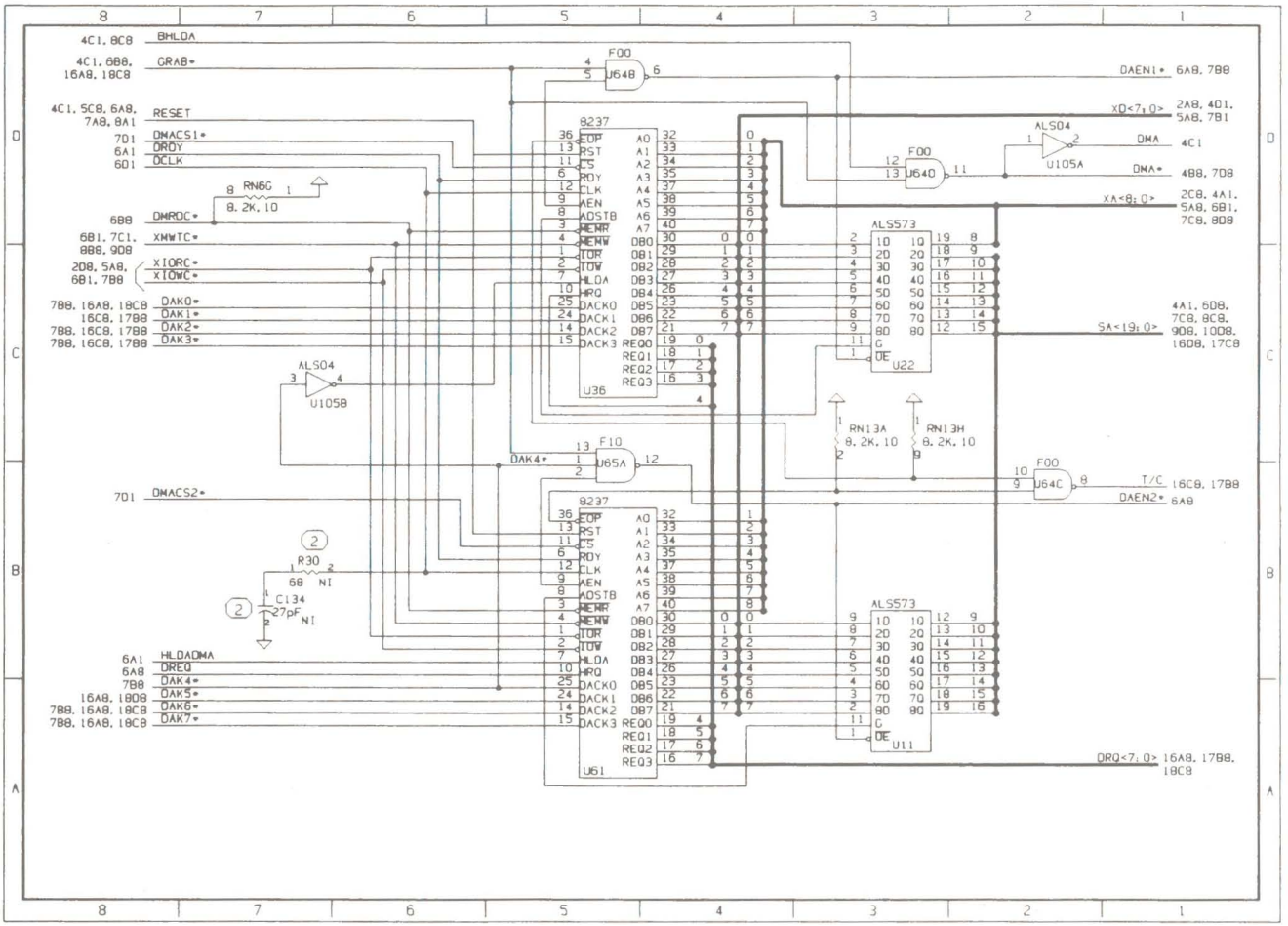


Figure 2-76. The 12 MHz DESKPRO 286 System Board Schematics (Page 3 of 19)

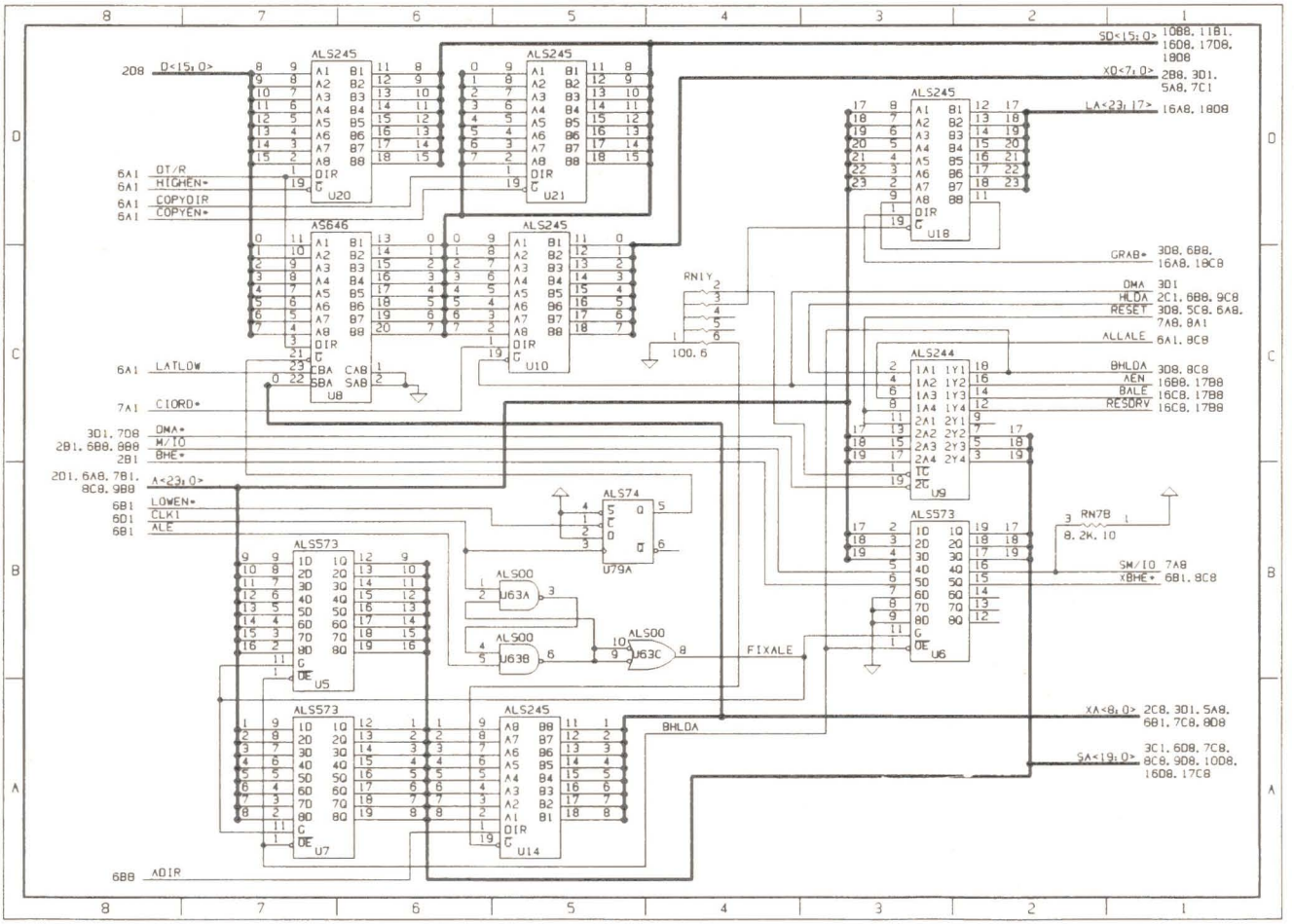


Figure 2-76. The 12 MHz DESKPRO 286 System Board Schematics (Page 4 of 19)

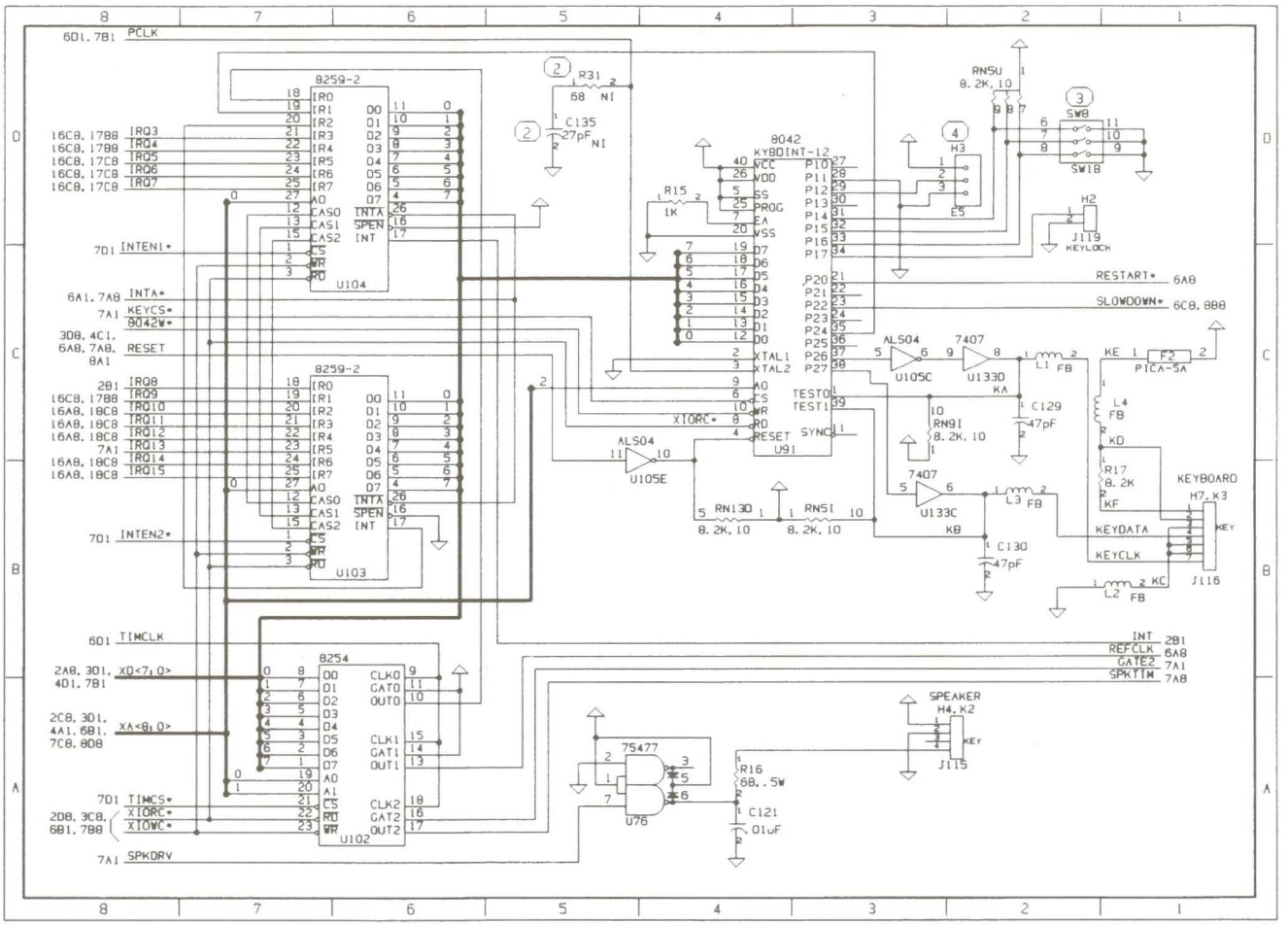


Figure 2-76. The 12 MHz DESKPRO 286 System Board Schematics (Page 5 of 19)

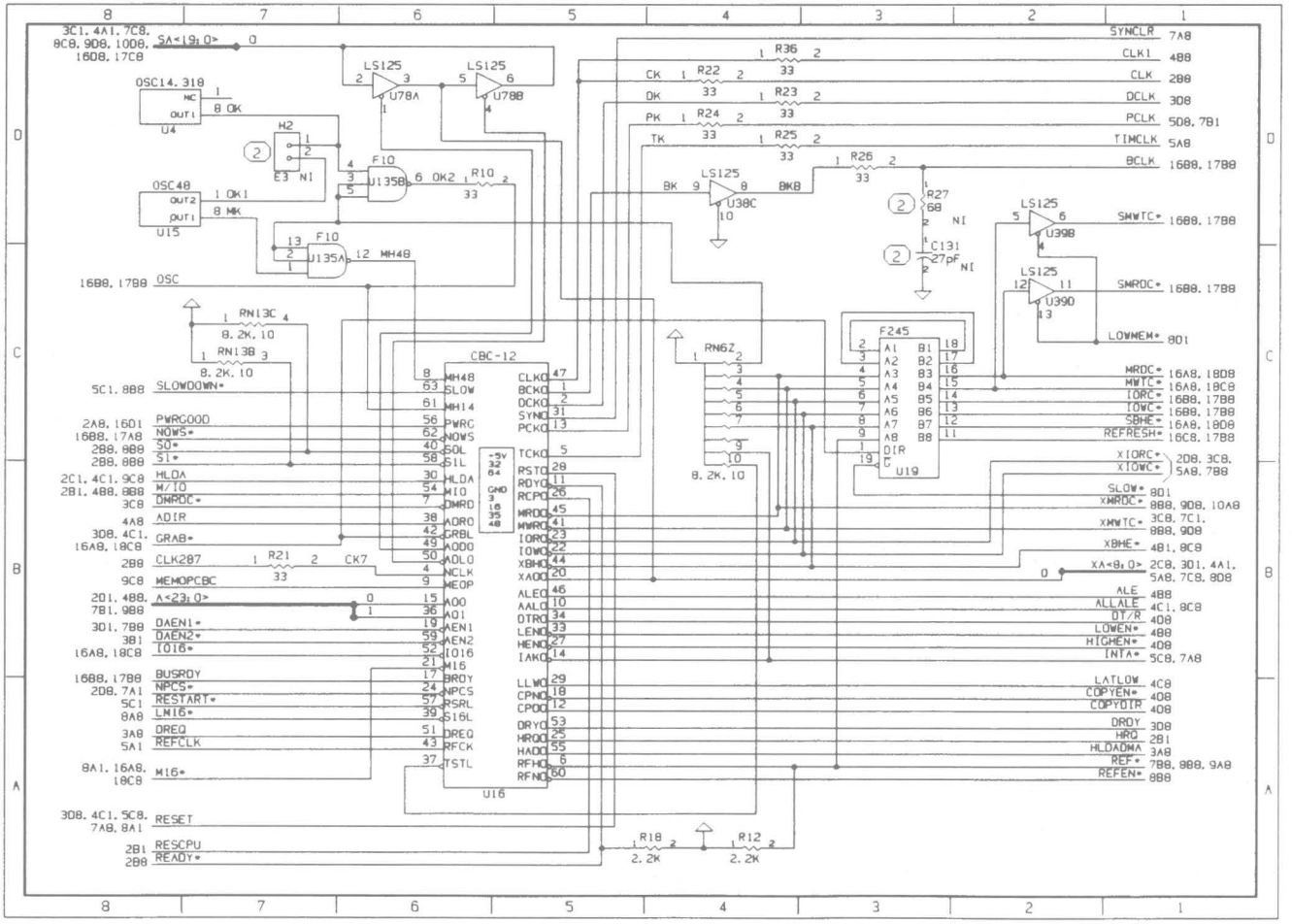


Figure 2-76. The 12 MHz DESKPRO 286 System Board Schematics (Page 6 of 19)

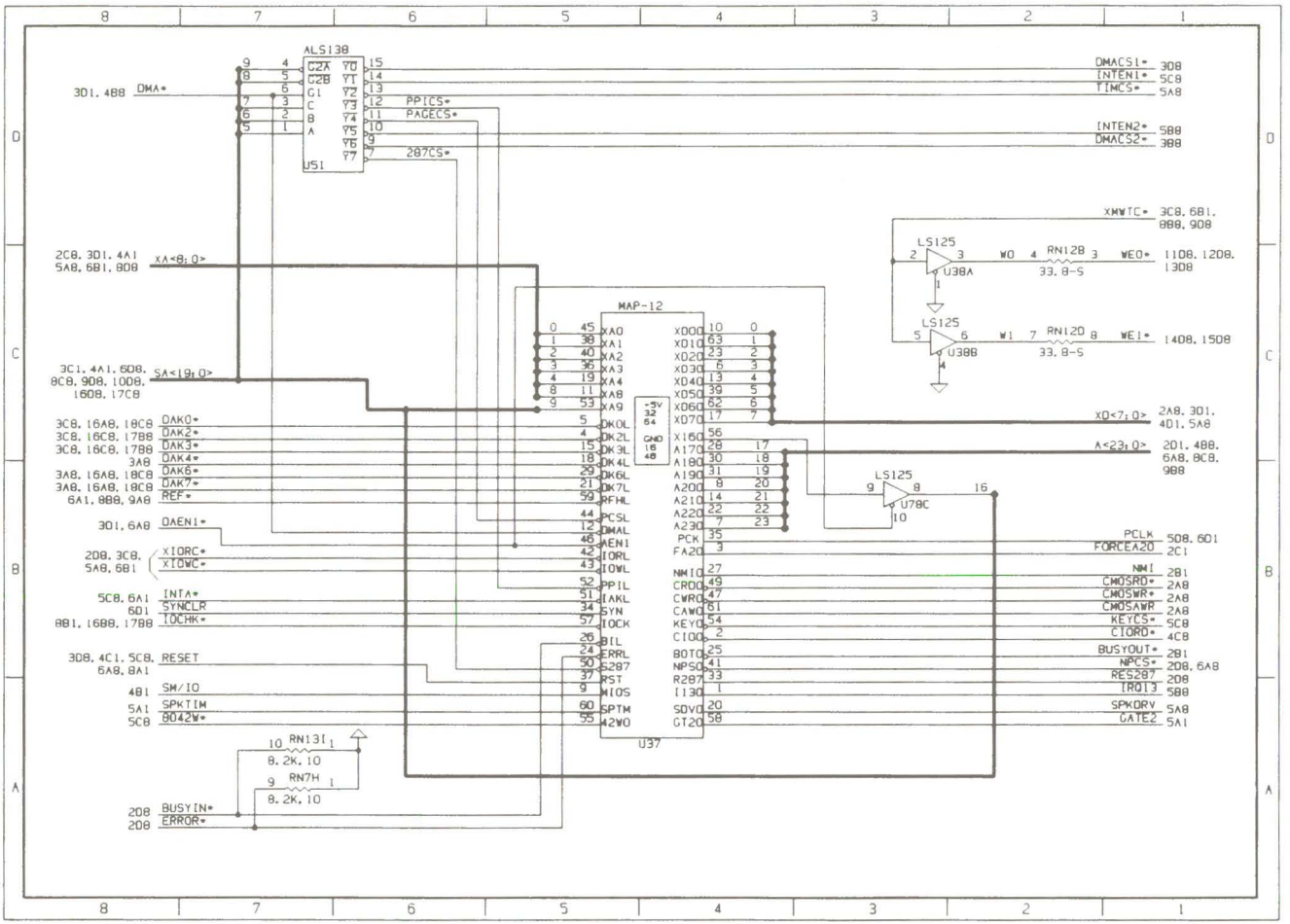


Figure 2-76. The 12 MHz DESKPRO 286 System Board Schematics (Page 7 of 19)

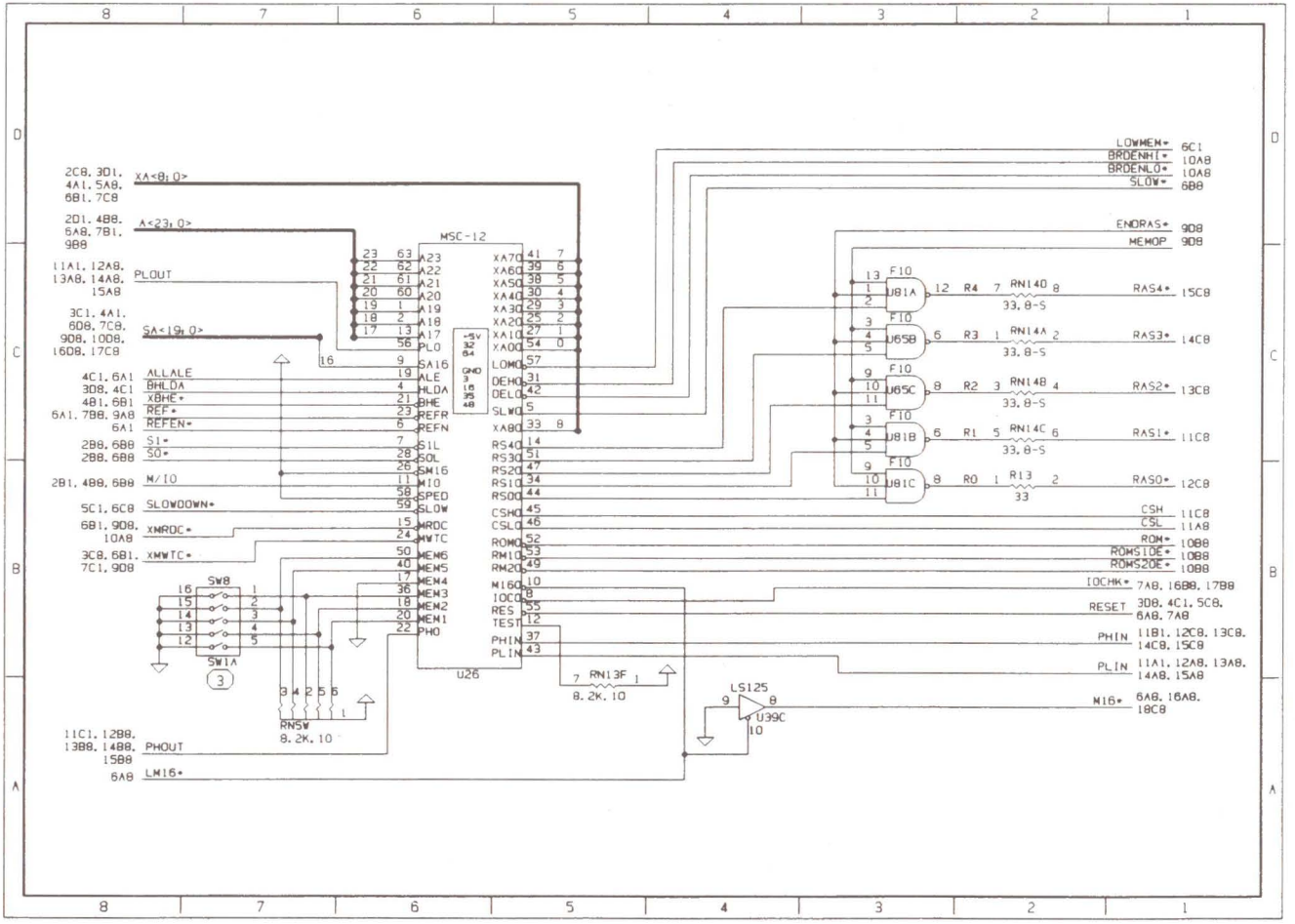


Figure 2-76. The 12 MHz DESKPRO 286 System Board Schematics (Page 8 of 19)

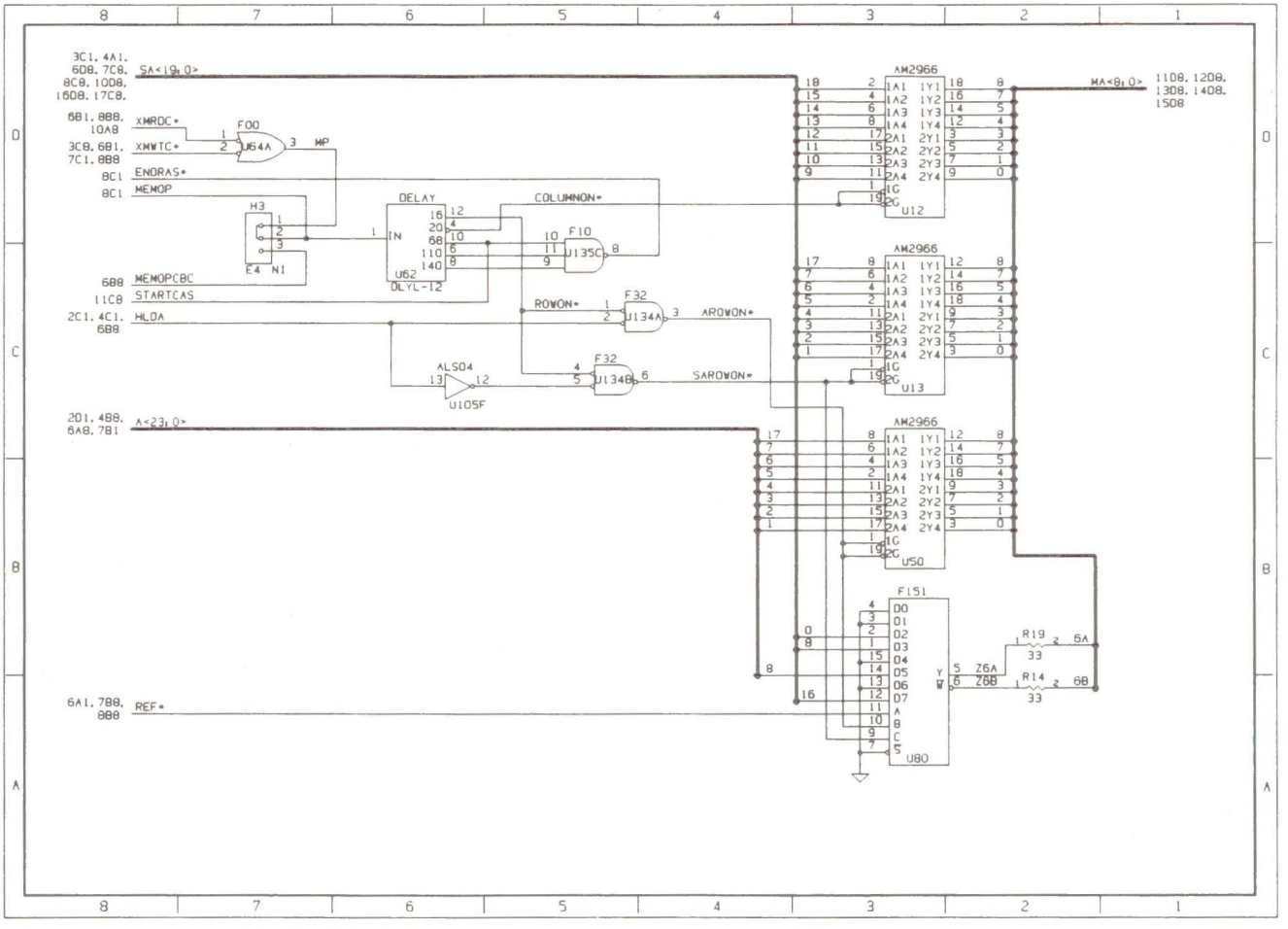


Figure 2-76. The 12 MHz DESKPRO 286 System Board Schematics (Page 9 of 19)

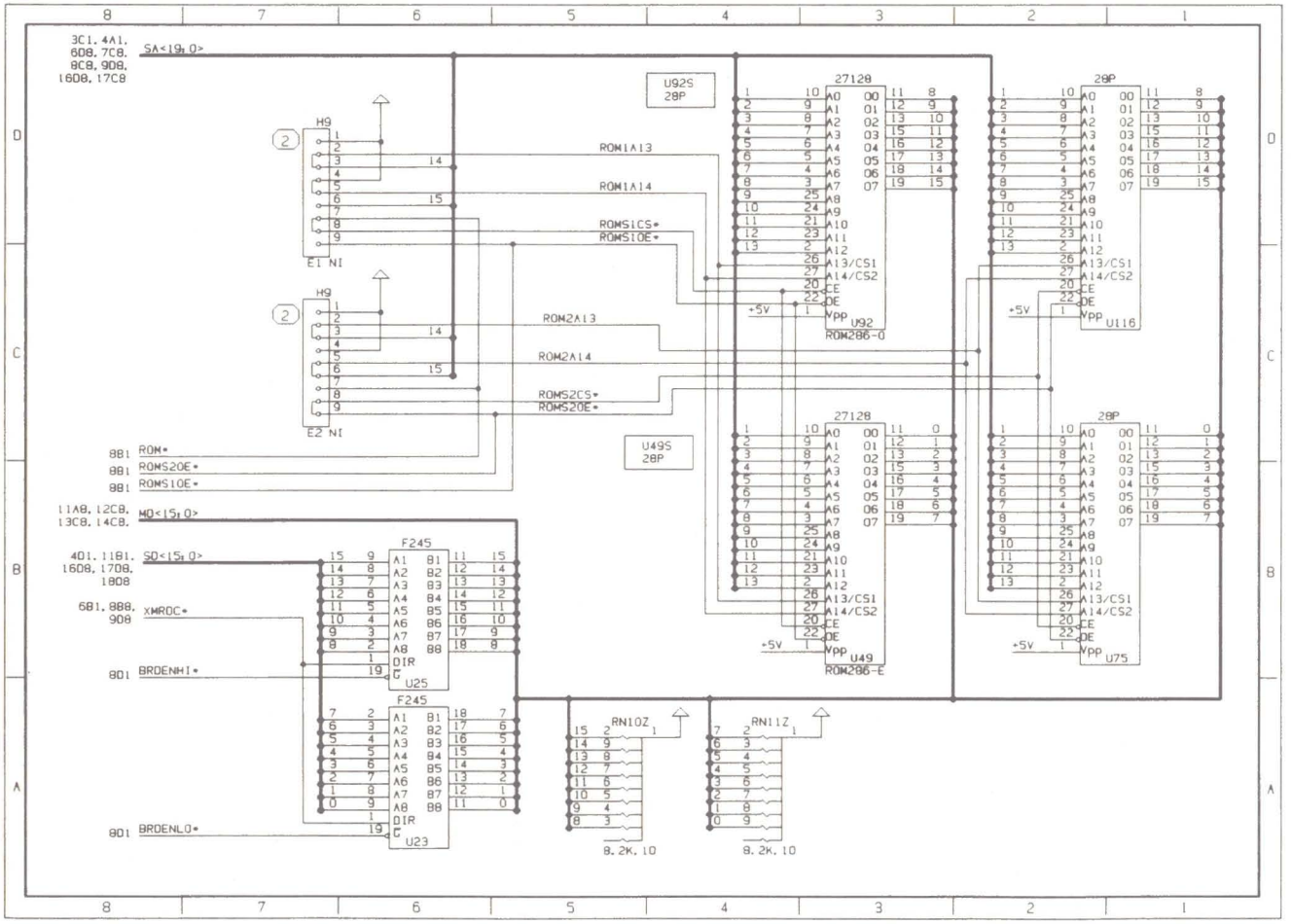


Figure 2-76. The 12 MHz DESKPRO 286 System Board Schematics (Page 10 of 19)

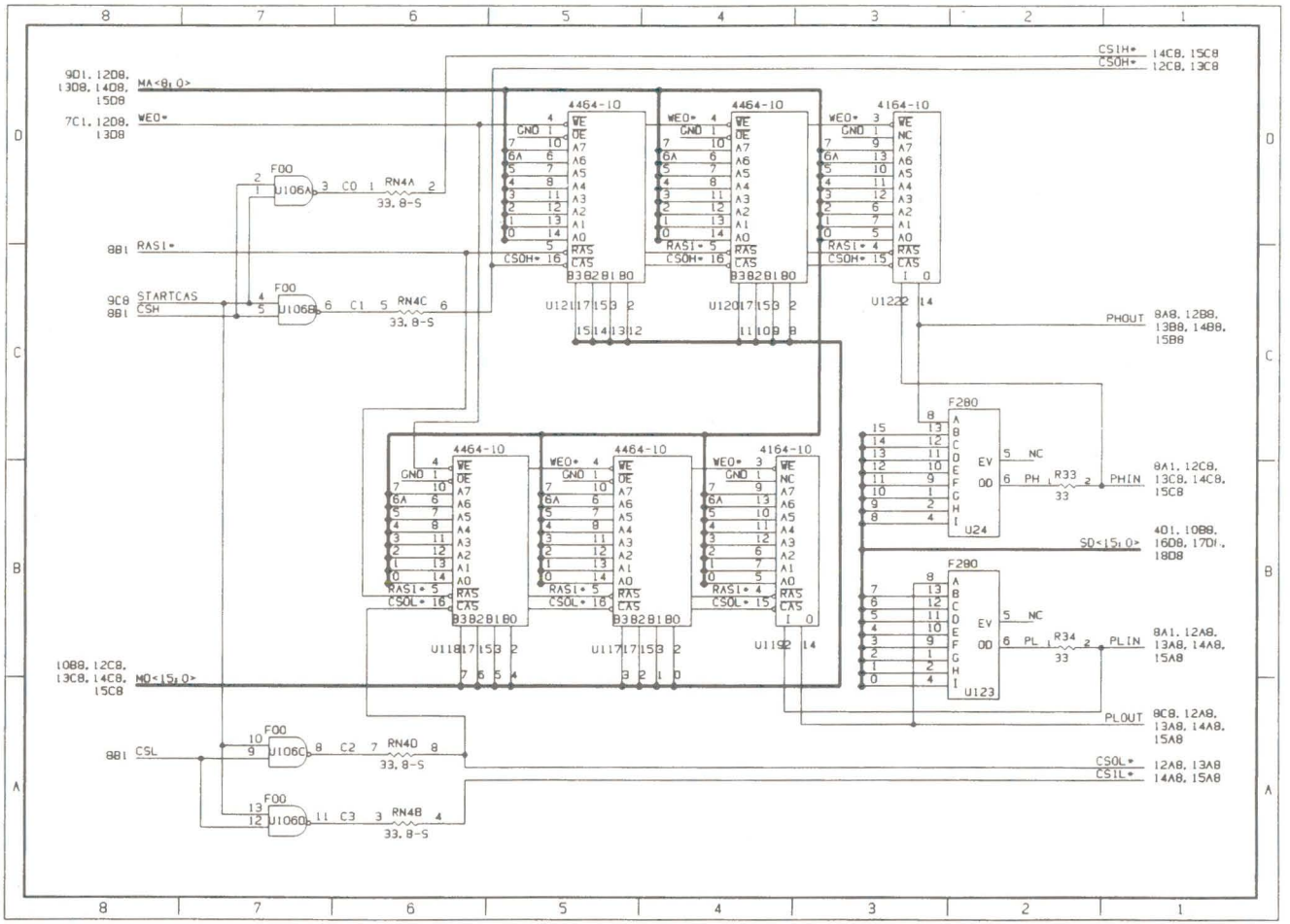


Figure 2-76. The 12 MHz DESKPRO 286 System Board Schematics (Page 11 of 19)

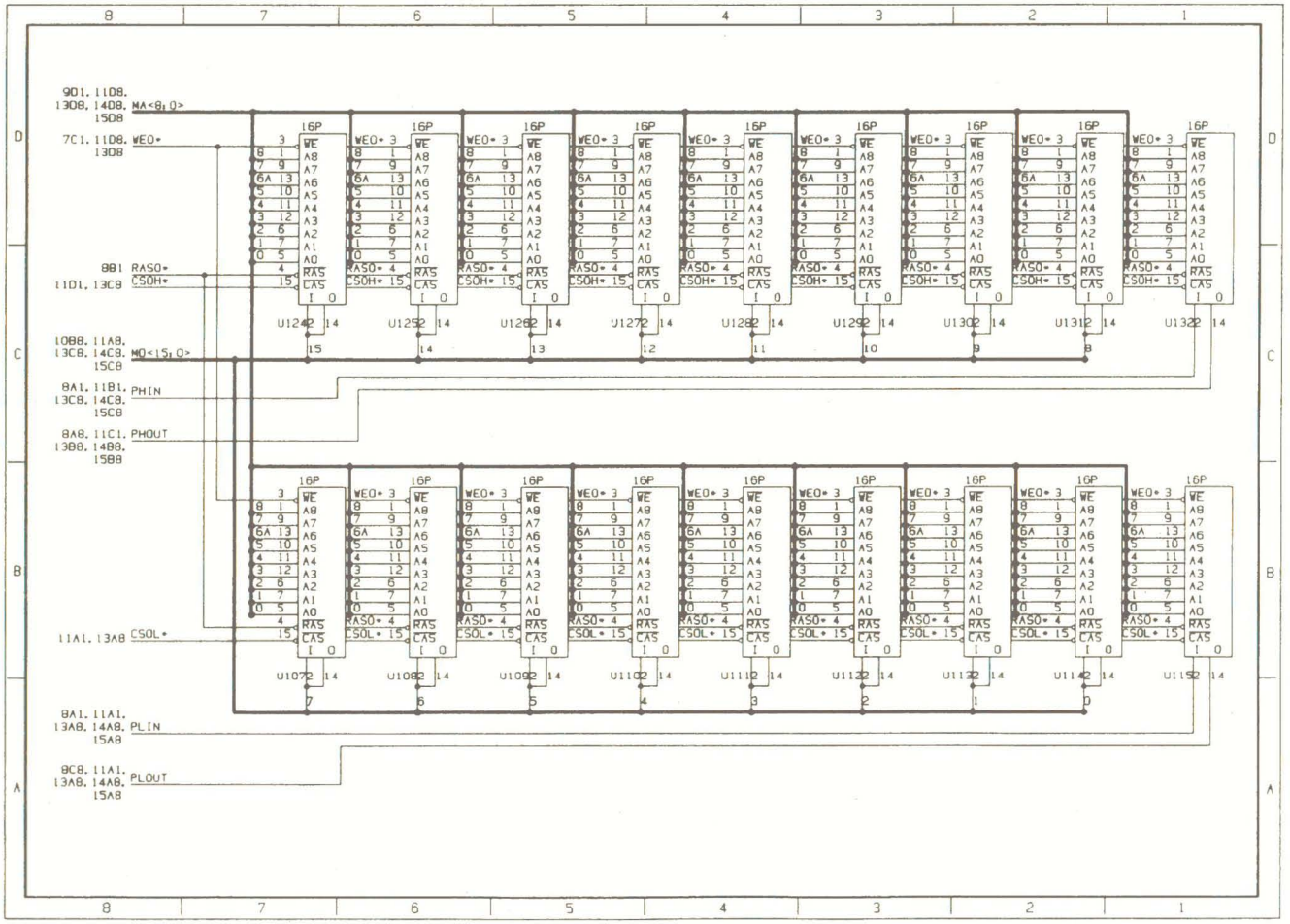


Figure 2-76. The 12 MHz DESKPRO 286 System Board Schematics (Page 12 of 19)

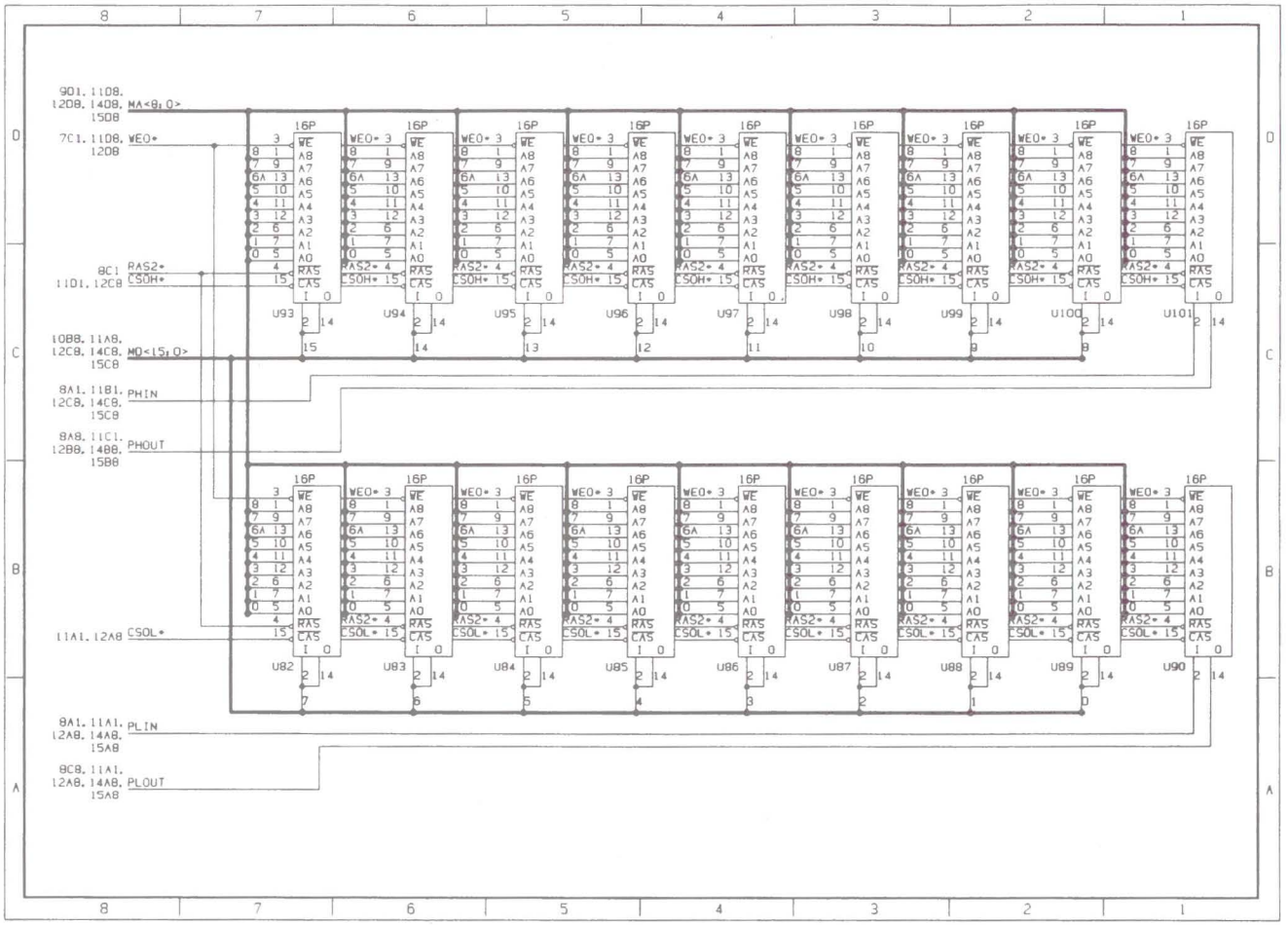


Figure 2-76. The 12 MHz DESKPRO 286 System Board Schematics (Page 13 of 19)

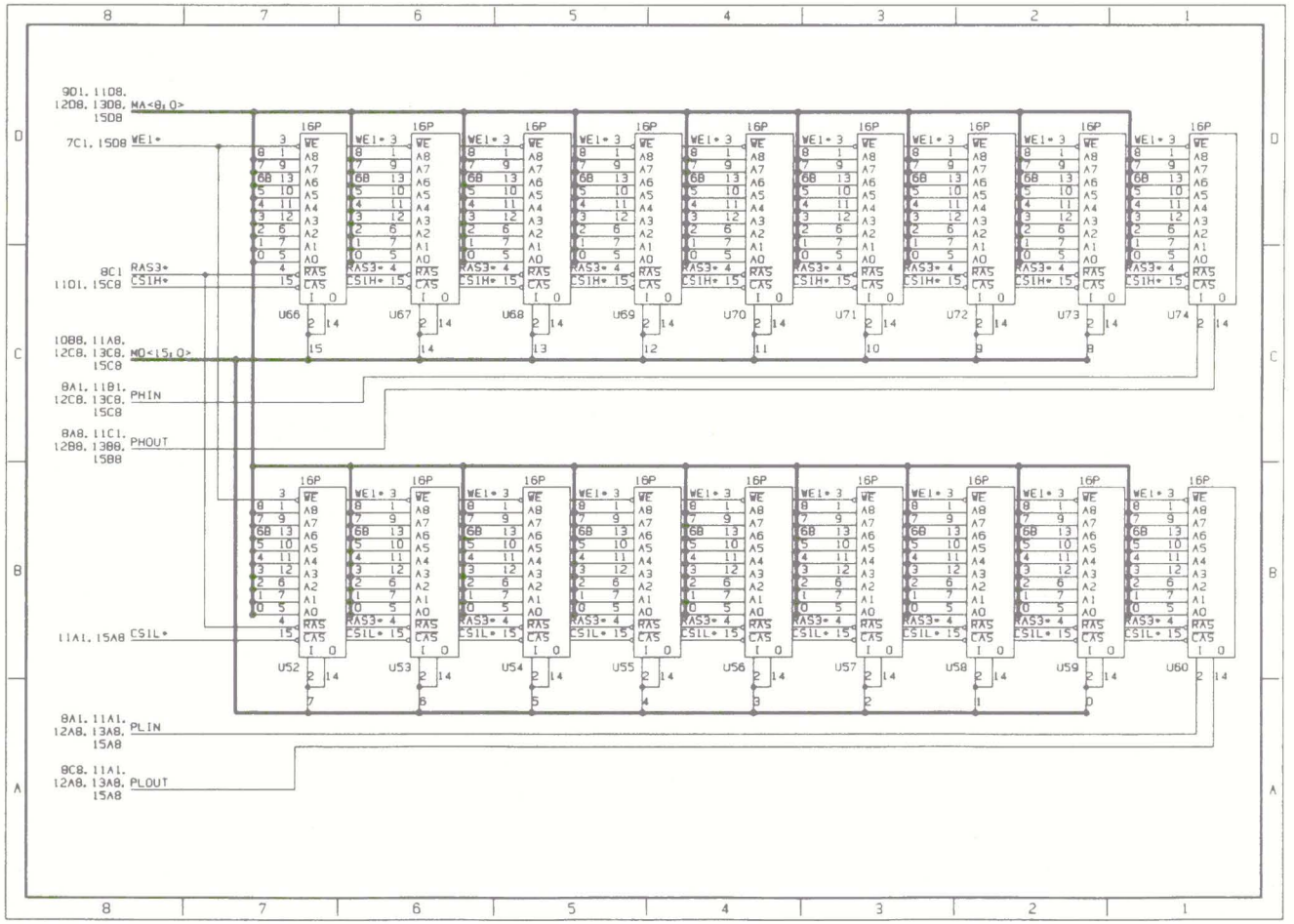


Figure 2-76. The 12 MHz DESKPRO 286 System Board Schematics (Page 14 of 19)

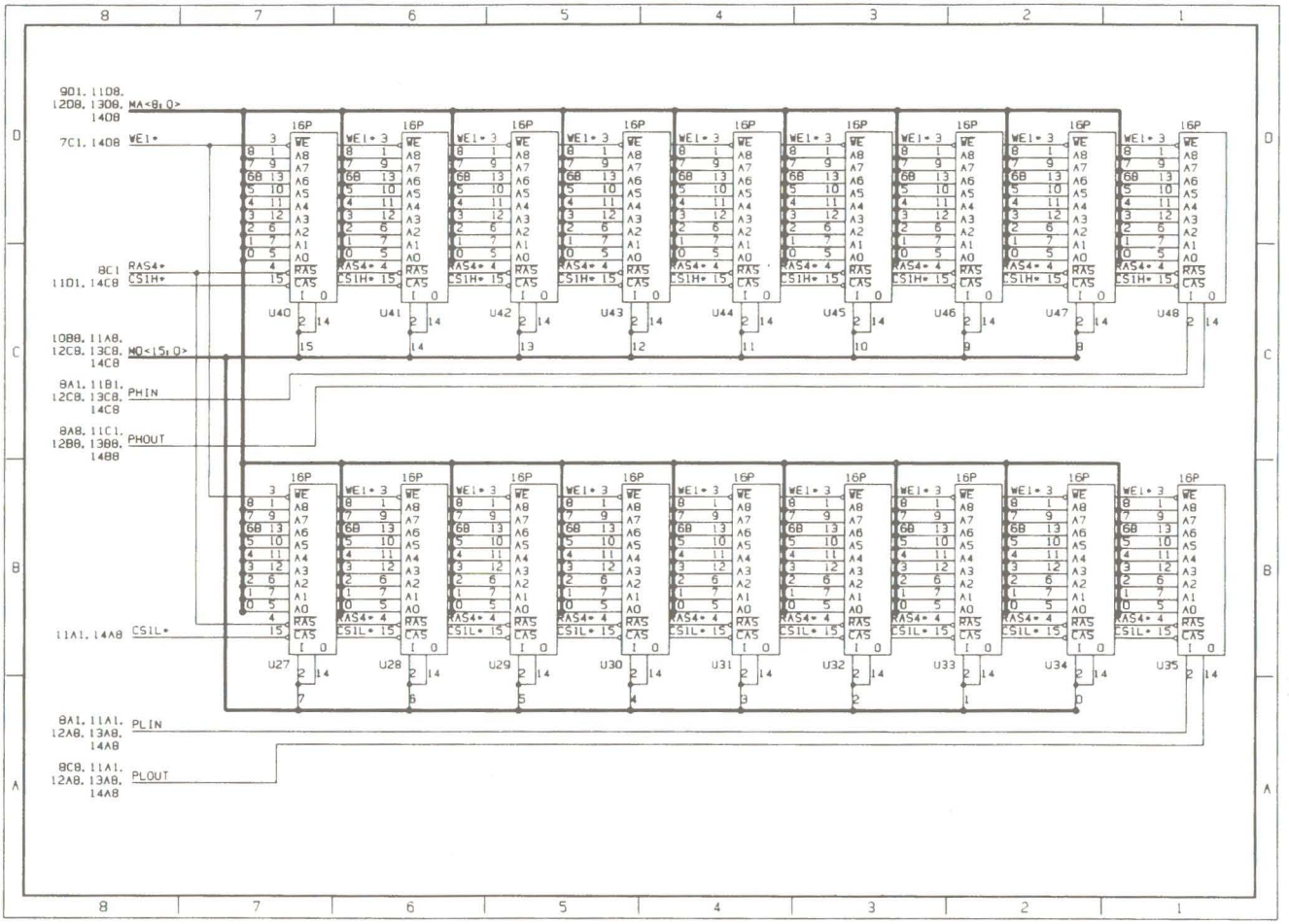


Figure 2-76. The 12 MHz DESKPRO 286 System Board Schematics (Page 15 of 19)

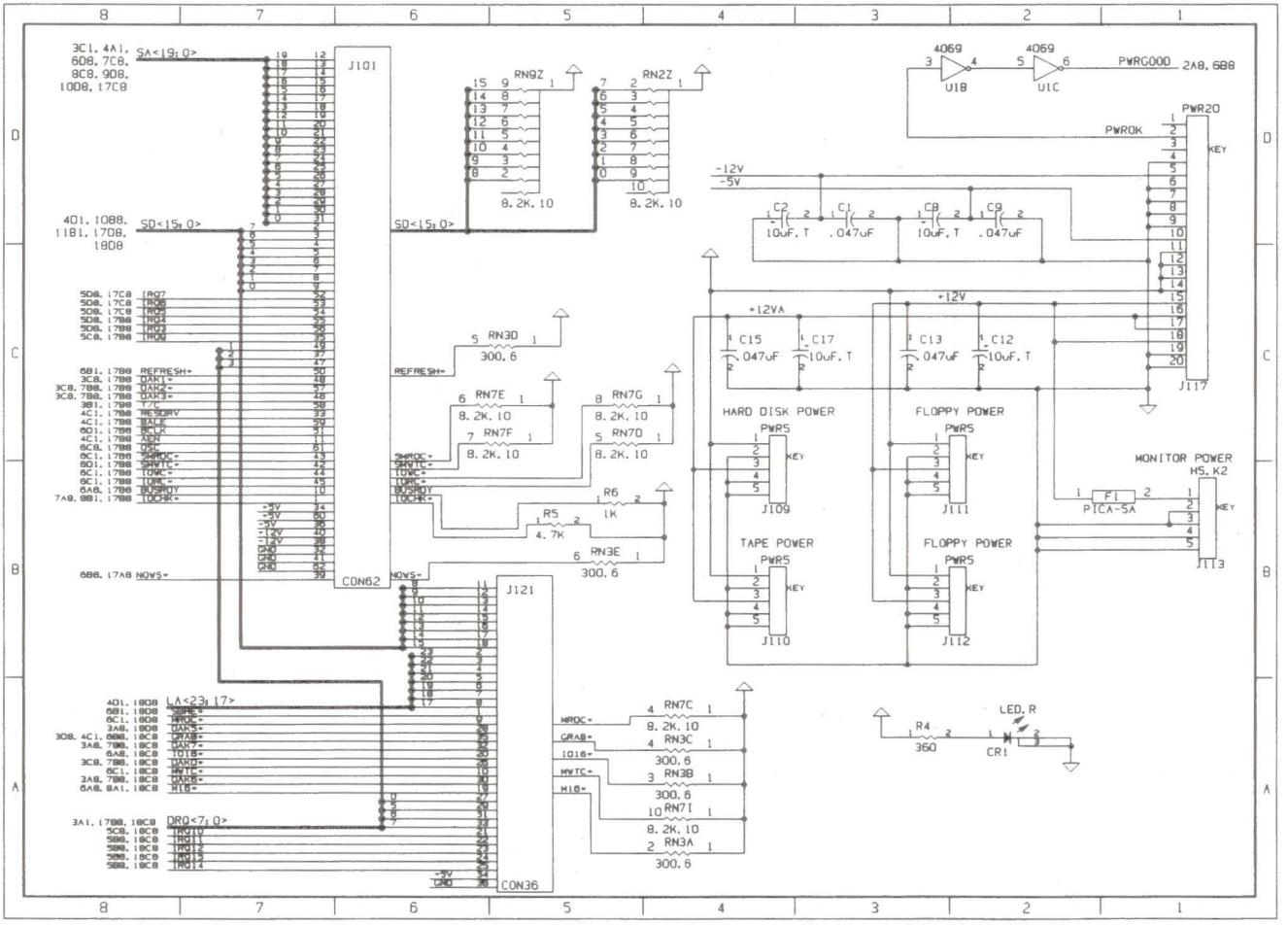


Figure 2-76. The 12 MHz DESKPRO 286 System Board Schematics (Page 16 of 19)

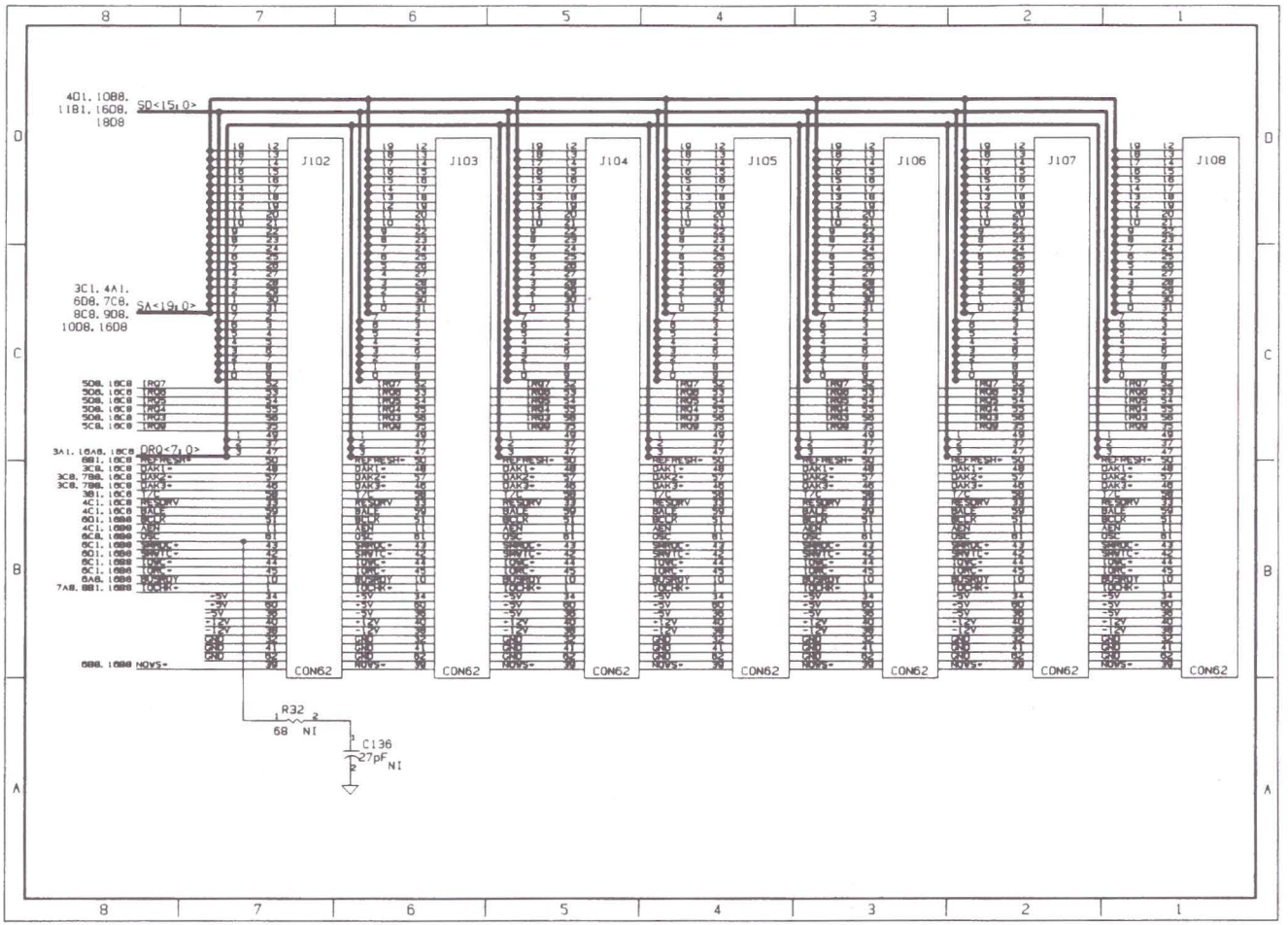


Figure 2-76. The 12 MHz DESKPRO 286 System Board Schematics (Page 17 of 19)

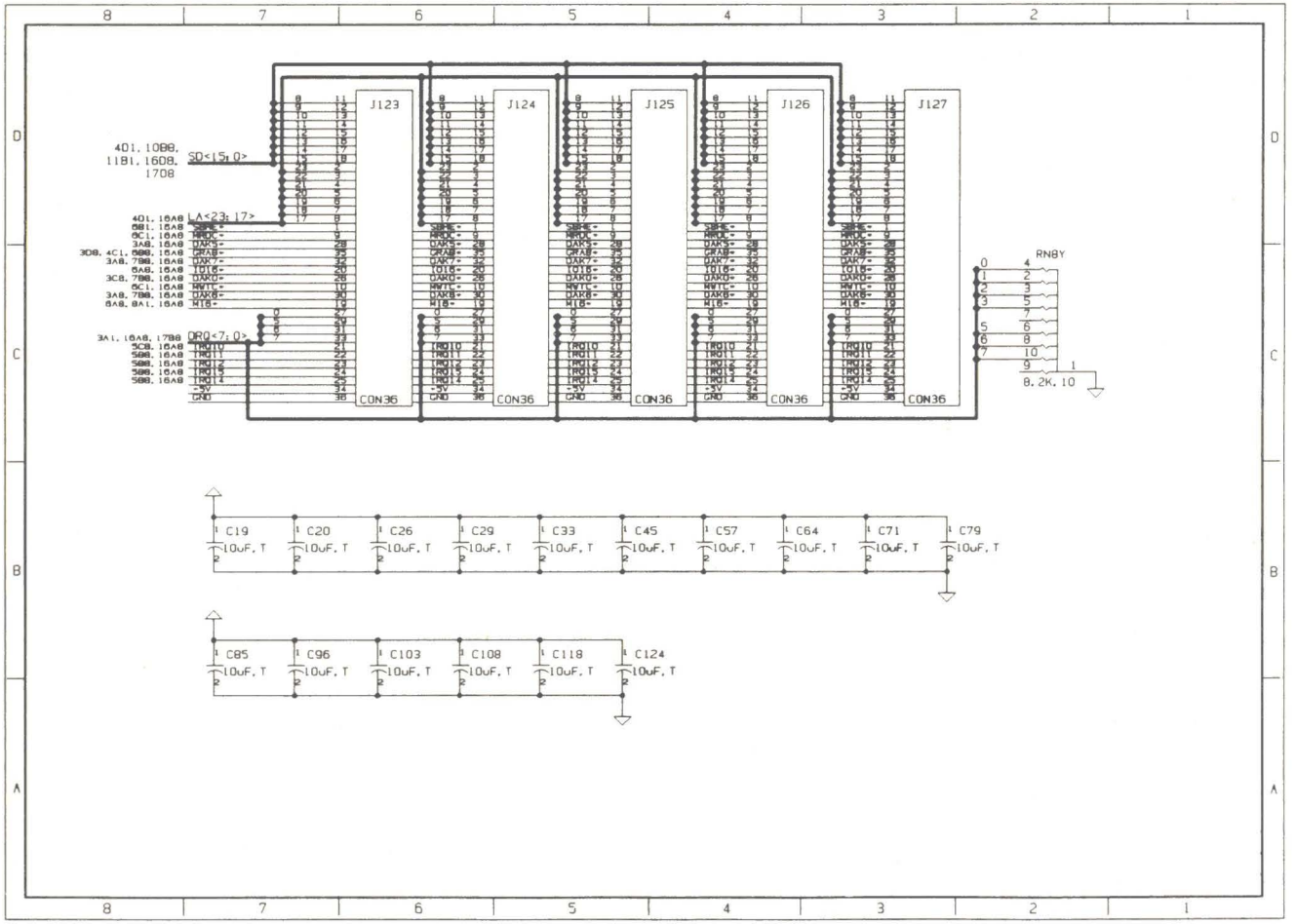


Figure 2-76. The 12 MHz DESKPRO 286 System Board Schematics (Page 18 of 19)

Figure 2-76. The 12 MHz DESKPRO 286 System Board Schematics (Page 19 of 19)

Chapter 3

COMPAQ DESKPRO 286 SYSTEM MEMORY BOARD

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CHAPTER 3
COMPAQ DESKPRO 286 SYSTEM MEMORY BOARD

Chapter 3
COMPAQ DESKPRO 286 System Memory Board

3.1 INTRODUCTION

The COMPAQ DESKPRO 286® Version 1 System Memory Board is required for use with the COMPAQ DESKPRO 286 Version 1 System Board. The System Memory Board provides system memory, ROM and RAM. Memory address decoding and memory support functions are described in Chapter 2, SYSTEM BOARD.

There are three versions of the COMPAQ DESKPRO 286 System Memory Board. All three boards are functionally equivalent. Version 1 can be distinguished from Versions 2 and 3 by component layout (see Figures 3-1 and 3-2). Versions 2 and 3 have the same component layout, but they have different assembly numbers. (See Figure 3-2 for location of assembly number). Version 2 has assembly number 000178-XXX and Version 3 has assembly number 000382-XXX.

Figures 3-1 and 3-2 show the component layout of the COMPAQ DESKPRO 286 System Memory Boards. Figure 3-3 shows the functional block diagram.

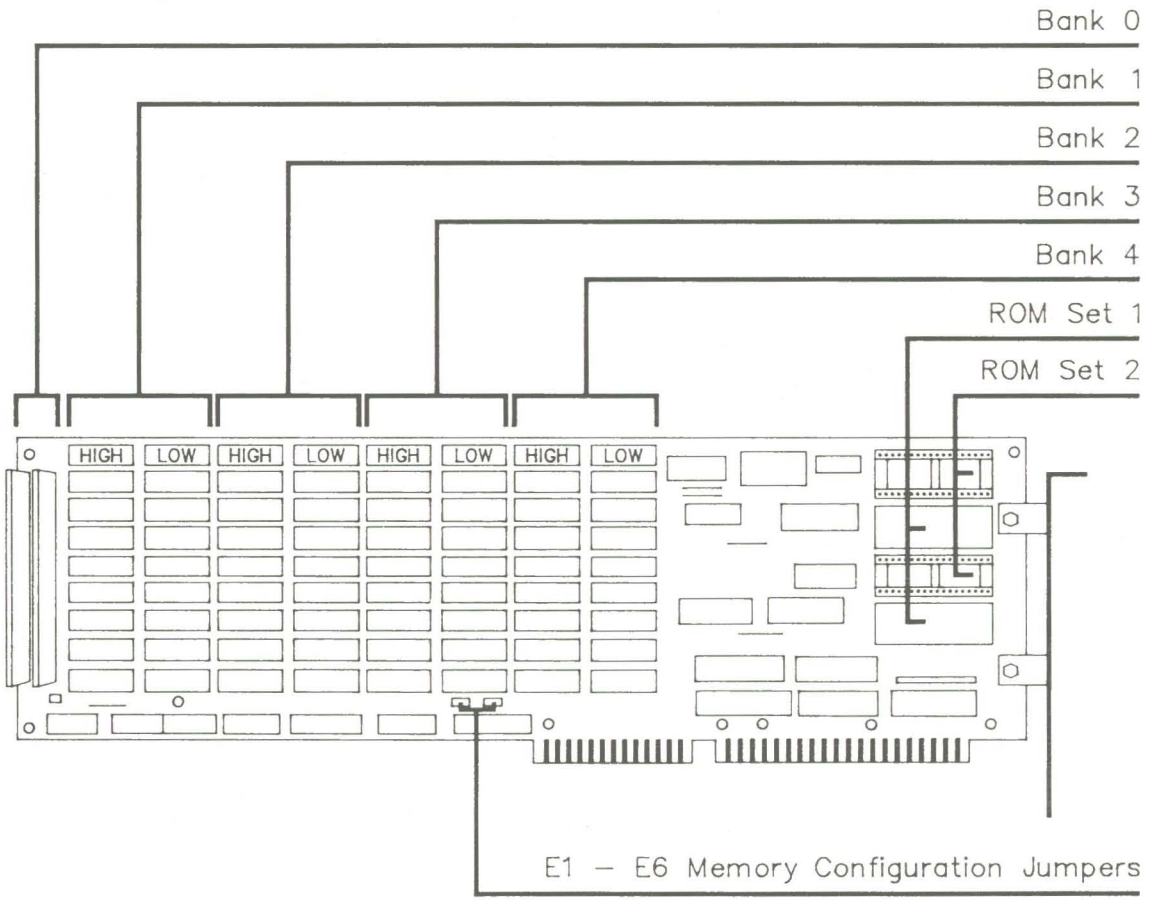


Figure 3-1. COMPAQ DESKPRO 286 System Memory Board Version 1 Component Layout

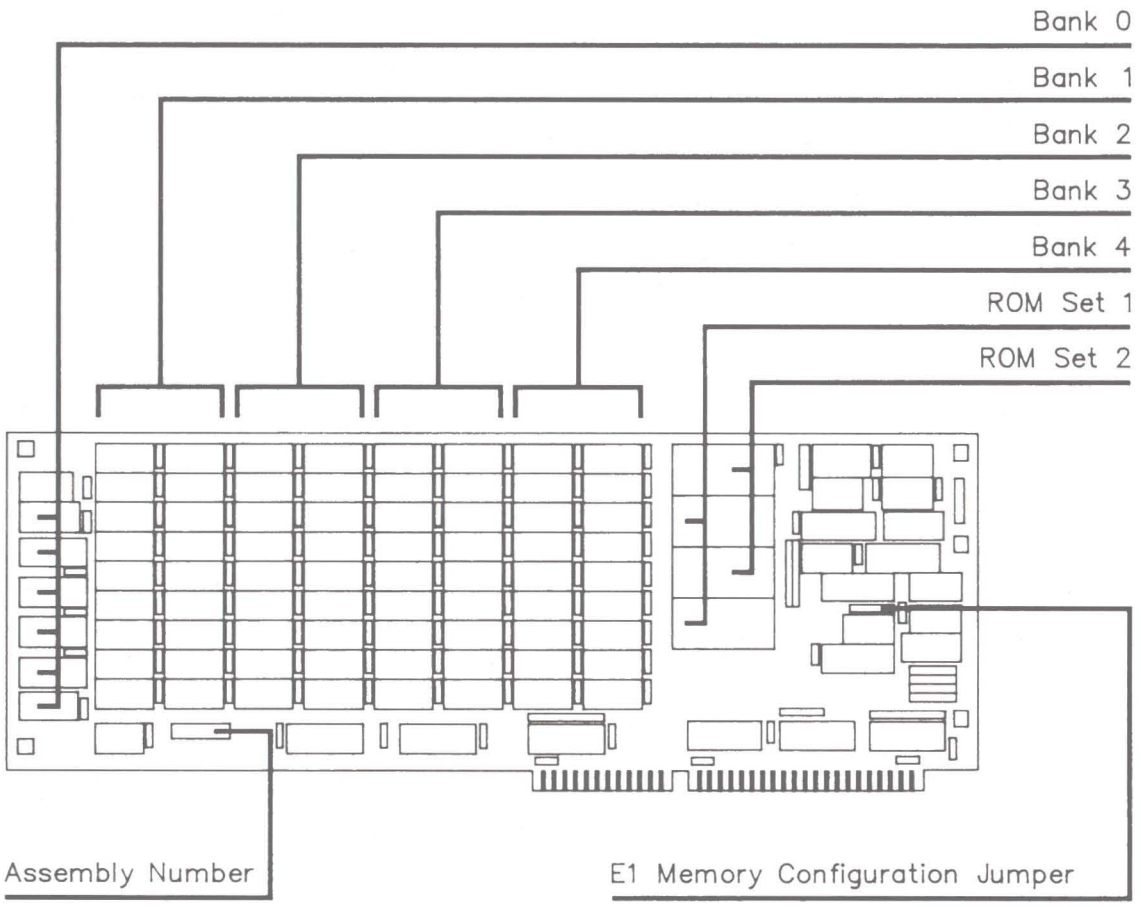


Figure 3-2. COMPAQ DESKPRO 286 System Memory Board Version 2 and Version 3 Component Layout

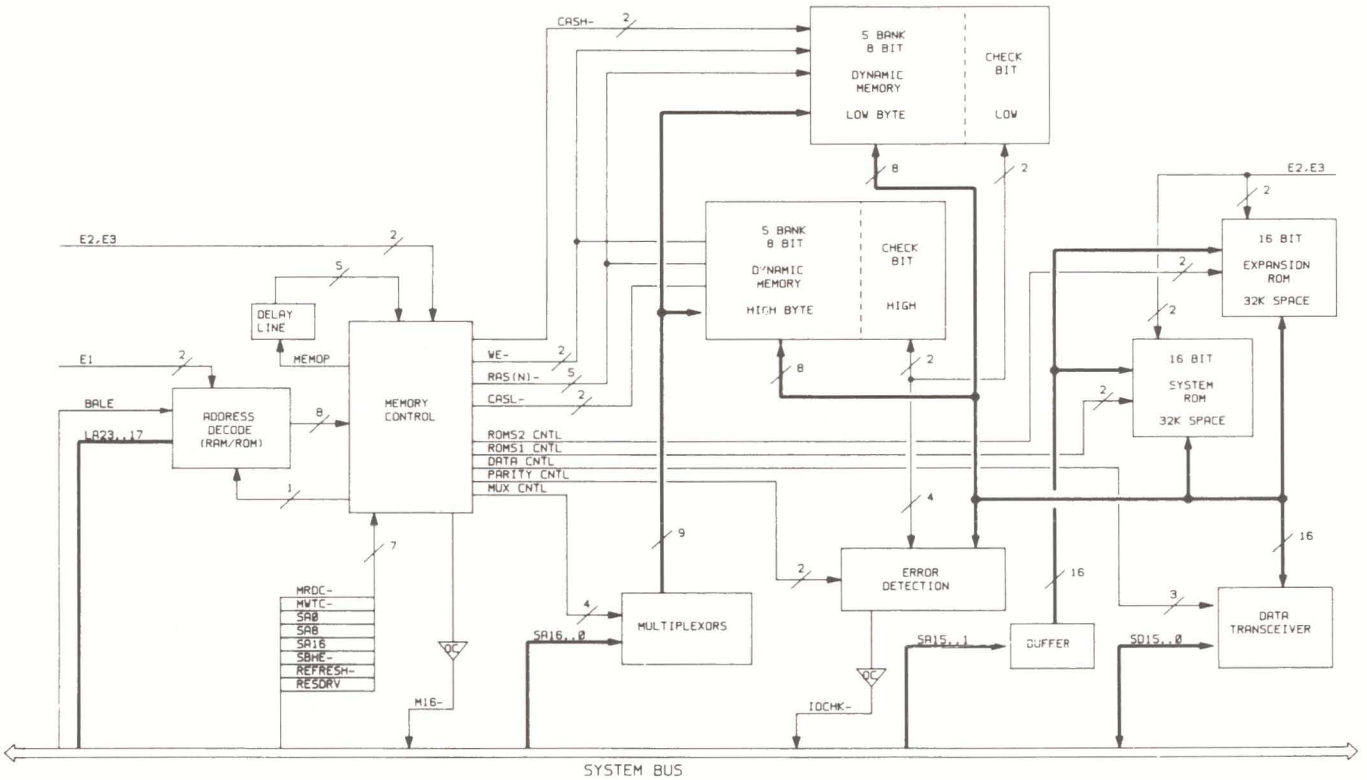


Figure 3-3. COMPAQ DESKPRO 286 System Memory Board Functional Block Diagram

3.2 COMPAQ DESKPRO 286 SYSTEM MEMORY BOARD RAM

NOTE: Memory address decoding and memory support are explained in Chapter 2.

The COMPAQ DESKPRO 286 System Memory Board has 128 Kbyte of RAM soldered in the first bank (Bank 0). The four remaining banks (Banks 1 through 4) are socketed so that either 64K x 1-bit or 256K x 1-bit RAM chips may be used. Memory must be expanded in full-bank increments (18 RAM chips) in contiguous and ascending order, using the same type of dynamic RAM (DRAM) devices.

Tables 3-1, 3-2, and 3-3 show the possible memory configurations and the corresponding jumper settings and address ranges for Versions 1, 2, and 3 of the System Memory Board respectively.

Table 3-1. Memory Configurations and Corresponding Jumper Settings Version 1

Jumper	Setting	Address Range	RAM Size	Bank 0	Bank 1	Bank 2	Bank 3	Bank 4
E1-E2	E5-E6	0-640 KB	64 KB	128 KB	128 KB	128 KB	128 KB	128 KB
E1-E2	E4-E5	0-512 KB	64 KB	128 KB	128 KB	128 KB	128 KB	(128 KB)
E2-E3	E5-E6	0-640 KB; 1-2.5MB	256 KB	128 KB	512 KB	512 KB	512 KB	512 KB
E2-E3	E4-E5	0-640 KB	256 KB	128 KB	512 KB	(512 KB)	(512 KB)	(512 KB)

Notes: 1. All memory sizes are in Kbytes unless otherwise noted.
2. Use the instructions that come with the COMPAQ memory option kit to properly configure your memory board.
3. Memory banks shown in parentheses ( ) are not enabled when the jumpers are set as shown, regardless of whether or not RAM is installed in these banks.

Table 3-2. Memory Configurations and Corresponding Jumper Settings Version 2

E1 Jumper Setting		Address Range	RAM Size	Bank 0	Bank 1	Bank 2	Bank 3	Bank 4
1-2	5-6	0-640 KB	64 KB	128 KB	128 KB	128 KB	128 KB	128 KB
1-2	4-5	0-512 KB	64 KB	128 KB	128 KB	128 KB	128 KB	(128 KB)
2-3	5-6	0-640 KB; 1-2.5MB	256 KB	128 KB	512 KB	512 KB	512 KB	512 KB
2-3	4-5	0-640 KB	256 KB	128 KB	512 KB	(512 KB)	(512 KB)	(512 KB)

Notes: 1. All memory sizes are in Kbytes unless otherwise noted.
2. Use the instructions that come with the COMPAQ memory option kit to properly configure your memory board.
3. Memory banks shown in parentheses ( ) are not enabled when the jumpers are set as shown, regardless of whether or not RAM is installed in these banks.

Table 3-3. Memory Configurations and Corresponding Jumper Settings Version 3

E1 Jumper Setting		Address Range	RAM Size	Bank 0	Bank 1	Bank 2	Bank 3	Bank 4
1-2	5-6	0-640 KB	64 KB	128 KB	128 KB	128 KB	128 KB	128 KB
1-2	4-5	0-512 KB	64 KB	128 KB	128 KB	128 KB	128 KB	(128 KB)
2-3	5-6	0-640 KB; 1-2.5MB	256 KB	128 KB	512 KB	512 KB	512 KB	512 KB
2-3	4-5	0-256 KB		128 KB	128 KB	(128 KB)	(128 KB)	(128 KB)

Notes: 1. All memory sizes are in Kbytes unless otherwise noted.
2. Use the instructions that come with the COMPAQ memory option kit to properly configure your memory board.
3. Memory banks shown in parentheses ( ) are not enabled when the jumpers are set as shown, regardless of whether or not RAM is installed in these banks.

There are five possible memory configurations for the COMPAQ DESKPRO 286 System Memory Board. Configurations 1 through 5 are supported by Versions 1 and 2. Configurations 1, 2, 3, and 5 are supported by Version 3.

1. 0-640 KB using 64K x 1-bit DRAM chips
2. 0-512 KB using 64K x 1-bit DRAM chips
3. 0-2.176 MB using 256K x 1-bit DRAM chips (0-640 KB plus 512 KB-1536 KB)
4. 0-640 KB using 256K x 1-bit DRAM chips
5. 0-256 KB using 64K x 1-bit DRAM chips

In every configuration, the lowest 128 Kbytes of RAM is permanently installed as Bank 0. Figure 3-4 and 3-5 shows the relationship between the memory map and the installed RAM banks for each configuration.

Configurations 2 and 5 are for use with certain hardware and software packages that require system memory to be limited. These configurations disable the specified address ranges without requiring removal of the unused RAM.

The system memory board uses COMPAQ-approved 64K x 1-bit or 256K x 1-bit DRAMs with a response time of 150 ns or faster. (CAS access time must be 75 ns or faster.)

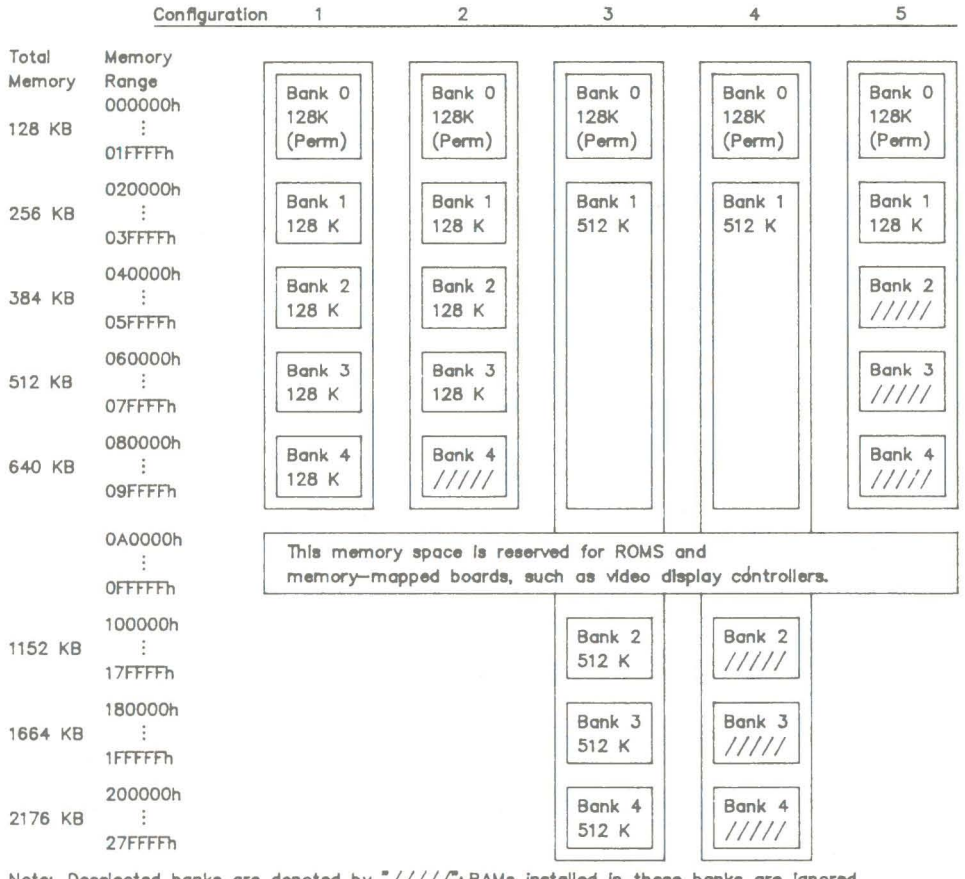


Figure 3-4. COMPAQ DESKPRO 286 (with Version 1 System Board) Memory Configurations

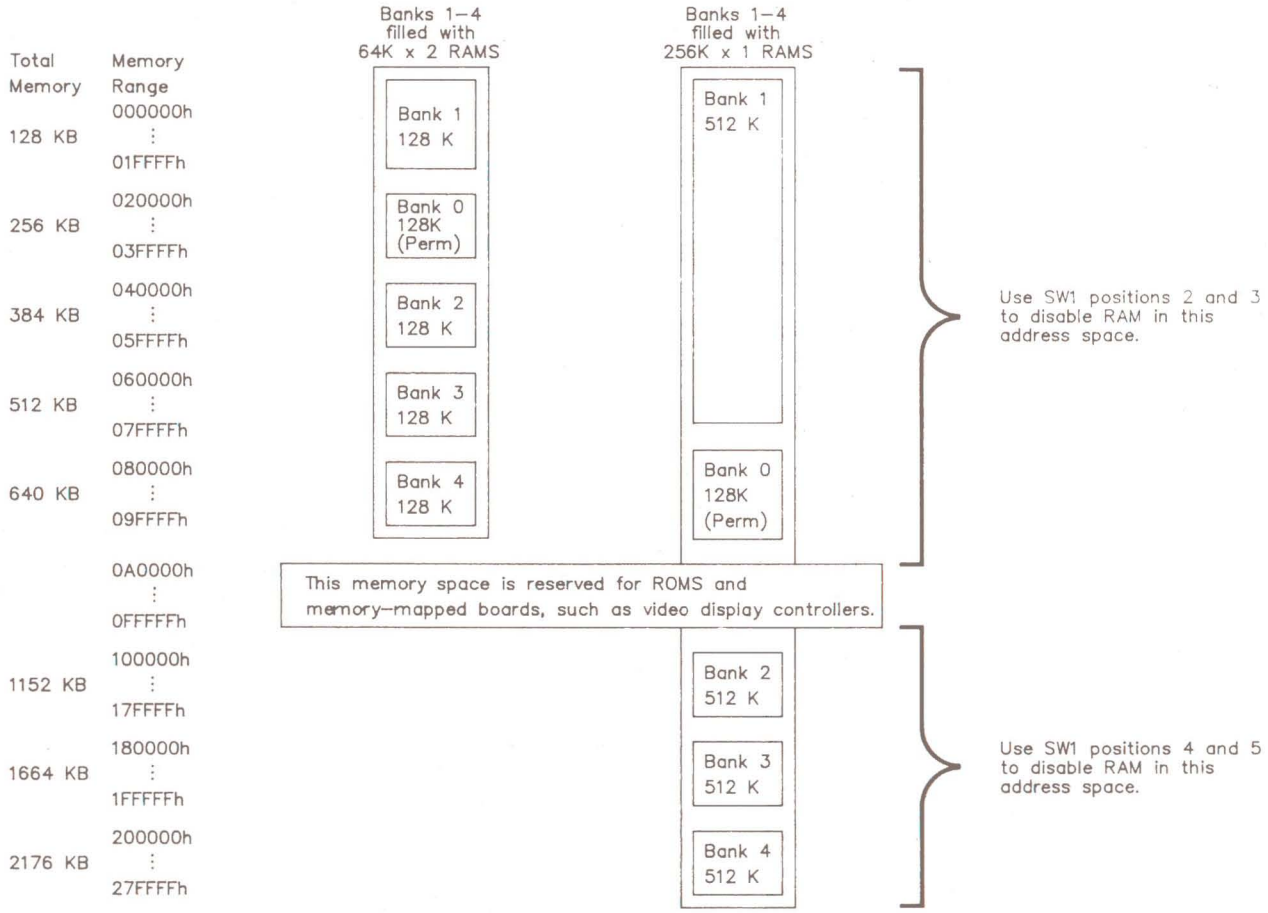


Figure 3-5. COMPAQ DESKPRO 286 (with Version 2 System Board) Memory Configurations

3.3 COMPAQ DESKPRO 286 SYSTEM MEMORY BOARD ROM

The COMPAQ DESKPRO System Memory Board has four 28-pin sockets for ROM or EPROM. The ROM sockets are addressed as two pairs, each 16 bits wide and designated as ROM Set 1 (always present and including address 0FFFF0h or FFFFF0h) and system ROM SET 2 (located in the address space 64 Kbytes below ROM Set 1).

ROM Set 1 controls the initial system operation (resetting and initializing the system). This code is known as the BIOS (Basic Input Output System). Installed in the two ROM Set 1 sockets are 16K x 8 devices, one containing all even bytes and the other containing all odd bytes. The two ROM Set 2 sockets are empty and are provided for future expansion.

ROMs can be, by pairs, either 8K x 8, 16K x 8, or 32K x 8 bits in size and can be either static or dynamic. ROM Set 1 occupies the 64-KB space at address 0F0000h through 0FEFFFh and identically at address FF0000h through FFFFFFh. ROM Set 2 occupies the 64-KB space at address 0E0000h through 0EFFFFh and identically at address FE0000h through FEFFFFh.

When 32K X 8 ROM chips are used, the pair of ROM chips fill the entire 64-Kbyte address space. When 16K x 8 ROM chips are used, the most-significant address bit is not decoded, so the ROM chips are double-mapped into two identical 32-Kbyte sections of the 64-Kbyte address space.

Similarly, when 8K x 8 ROMs are used, the two most-significant address bits are not decoded, so the ROM chips are quadruple-mapped into four identical 16-Kbyte sections of the 64-Kbyte address space.

3.4 JUMPERS

Several jumpers are provided to enable use of a variety of types of ROM for special applications.

Tables 3-4 and 3-5 lists the jumper settings and resulting configuration for each type of ROM.

Table 3-4. Jumper Settings for ROM Sets 1 and 2 - Version 1 System Memory Board

ROM Set 1 Jumper Settings			ROM Type
E7-E8	E10-E11	E13-E14	8Kx8, Static ROM, 250 ns
E8-E9	E10-E11	E13-E14	16Kx8, Static ROM, 250 ns
E7-E8	E11-E12	E13-E14	Invalid
E8-E9	E11-E12	E13-E14	32Kx8, Static ROM, 250 ns
E7-E8	E10-E11	E14-E15	8Kx8, Dynamic ROM, 150 ns
E8-E9	E10-E11	E14-E15	16Kx8, Dynamic ROM, 150 ns
E7-E8	E11-E12	E14-E15	Invalid
E8-E9	E11-E12	E14-E15	32Kx8, Dynamic ROM, 150 ns
ROM Set 2 Jumper Settings			**ROM Type**
E16-E17	E19-E20	E22-E23	8Kx8, Static ROM, 250 ns
E17-E18	E19-E20	E22-E23	16Kx8, Static ROM, 250 ns
E16-E17	E20-E21	E22-E23	Invalid
E17-E18	E20-E21	E22-E23	32Kx8, Static ROM, 250 ns
E16-E17	E19-E20	E23-E24	8Kx8, Dynamic ROM, 150 ns
E17-E18	E19-E20	E23-E24	16Kx8, Dynamic ROM, 150 ns
E16-E17	E20-E21	E23-E24	Invalid
E17-E18	E20-E21	E23-E24	32Kx8, Dynamic ROM, 150 ns

Table 3-5. Jumper Settings for ROM Sets 1 and 2 - Version 2 and 3 System Memory Board

ROM Set 1 - E2 ROM Set 2 - E3 Jumper Settings			ROM Type
1-2	4-5	7-8	8Kx8, Static ROM, 250 ns
2-3	4-5	7-8	16Kx8, Static ROM, 250 ns
1-2	5-6	7-8	Invalid
2-3	5-6	7-8	32Kx8, Static ROM, 250 ns
1-2	4-5	8-9	8Kx8, Dynamic ROM, 150 ns
2-3	4-5	8-9	16Kx8, Dynamic ROM, 150 ns
1-2	5-6	8-9	Invalid
2-3	5-6	8-9	32Kx8, Dynamic ROM, 150 ns

There are no jumper headers installed. The jumpers are etched on the solder side (bottom) of the board in the following configurations:

Version 1
ROM Set 1: 16K x 8 Static ROM (E8-E9, E10-E11, E13-E14)
ROM Set 2: 32K x 8 Dynamic ROM (E17-E18,E20-E21, E23-E24)

Version 2
ROM Set 1: 16K x 8 Static ROM (E1: 2-3, 4-5, 7-8)
ROM Set 2: 32K x 8 Dynamic ROM (E2: 2-3, 5-6, 8-9)

Changing the jumper settings requires cutting the conductor on the solder side (bottom) of the board to disconnect any unwanted jumpers, then soldering the wire(s) to jumpers as desired.

NOTE: Modifying these jumpers invalidates the COMPAQ warranty for this board.

3.5 SCHEMATICS

Figure 3-6 shows the schematics for the COMPAQ DESKPRO 286 System Memory Board Version 1. Figure 3-7 shows the schematics for the COMPAQ DESKPRO 286 System Memory Board Versions 2 and 3. Versions 2 and 3 have the same schematics, only the PALS are different. Compaq Computer Corporation does not guarantee the accuracy of the schematics. They are provided to aid in a general understanding of the system operation.

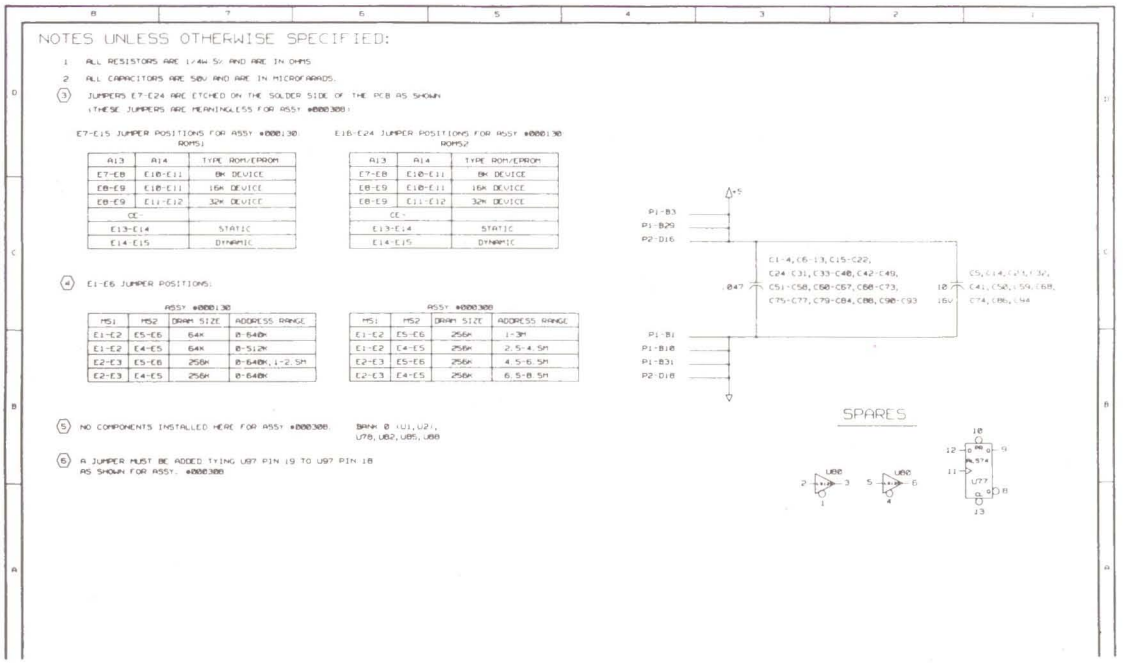


Figure 3-6. COMPAQ DESKPRO 286 System Memory Board Version 1 Schematics (Page 1 of 5)

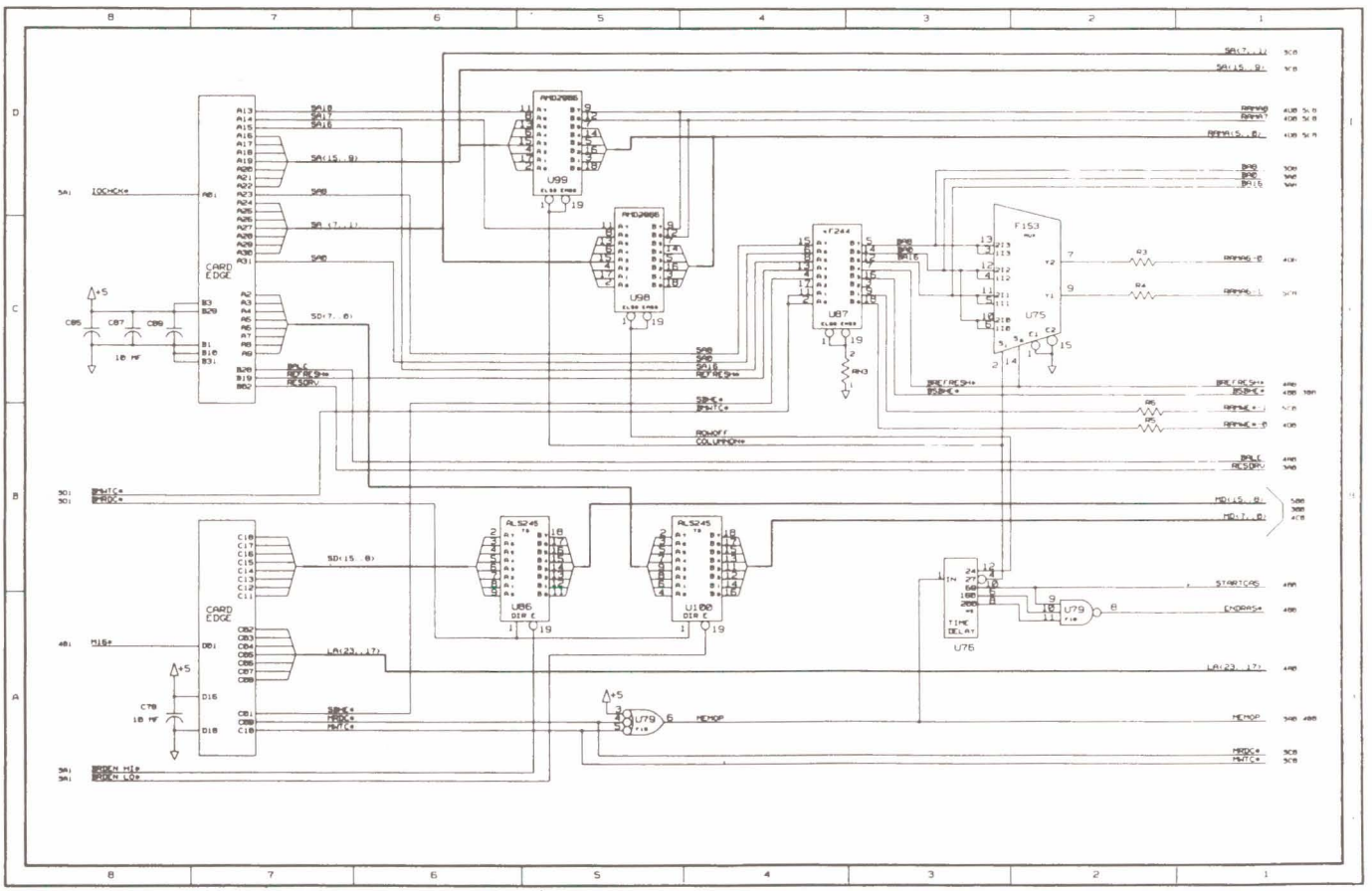


Figure 3-6. COMPAQ DESKPRO 286 System Memory Board Schematics (Page 2 of 5)

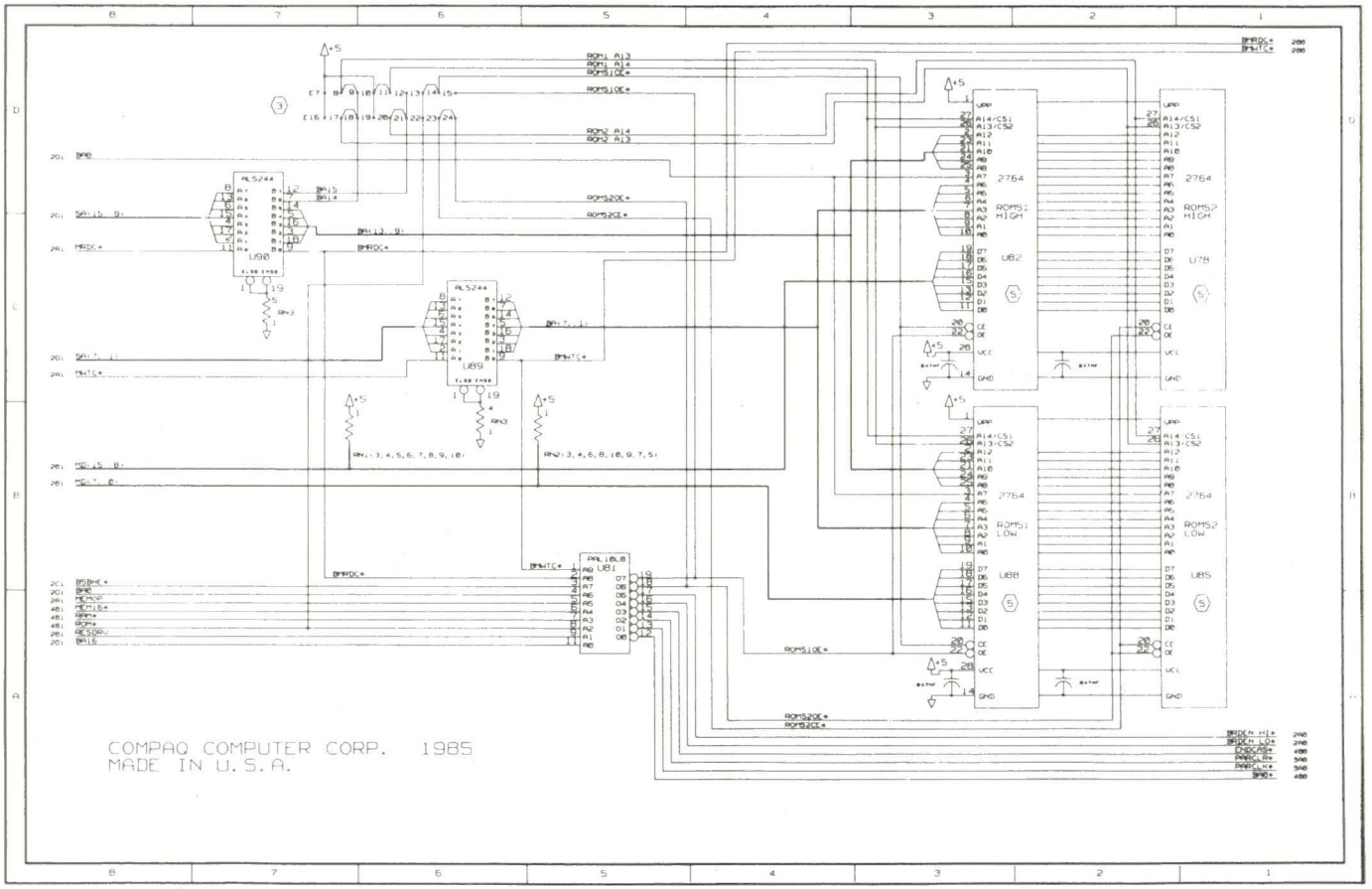


Figure 3-6. COMPAQ DESKPRO 286 System Memory Board Schematics (Page 3 of 5)

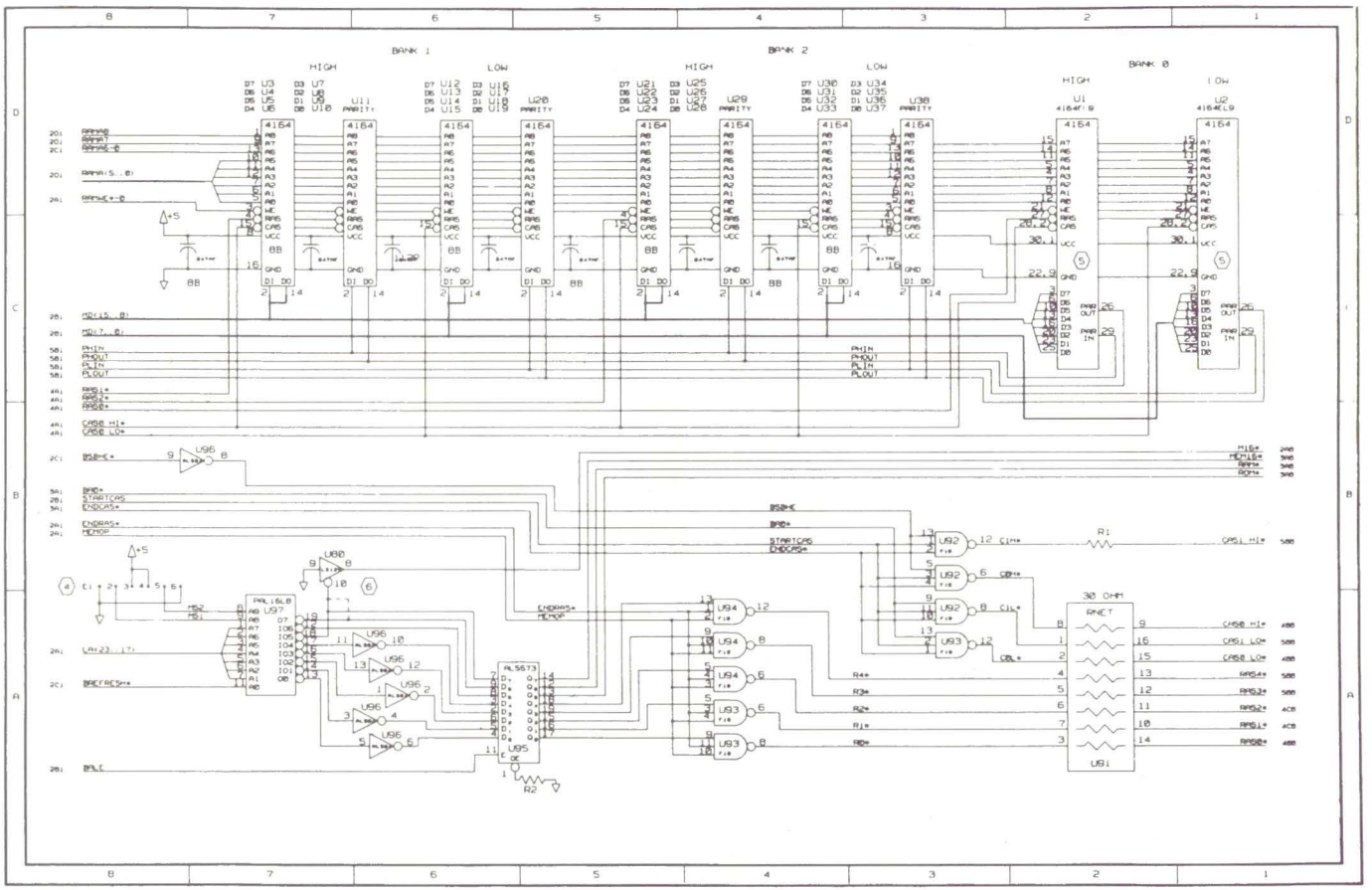


Figure 3-6. COMPAQ DESKPRO 286 System Memory Board Schematics (Page 4 of 5)

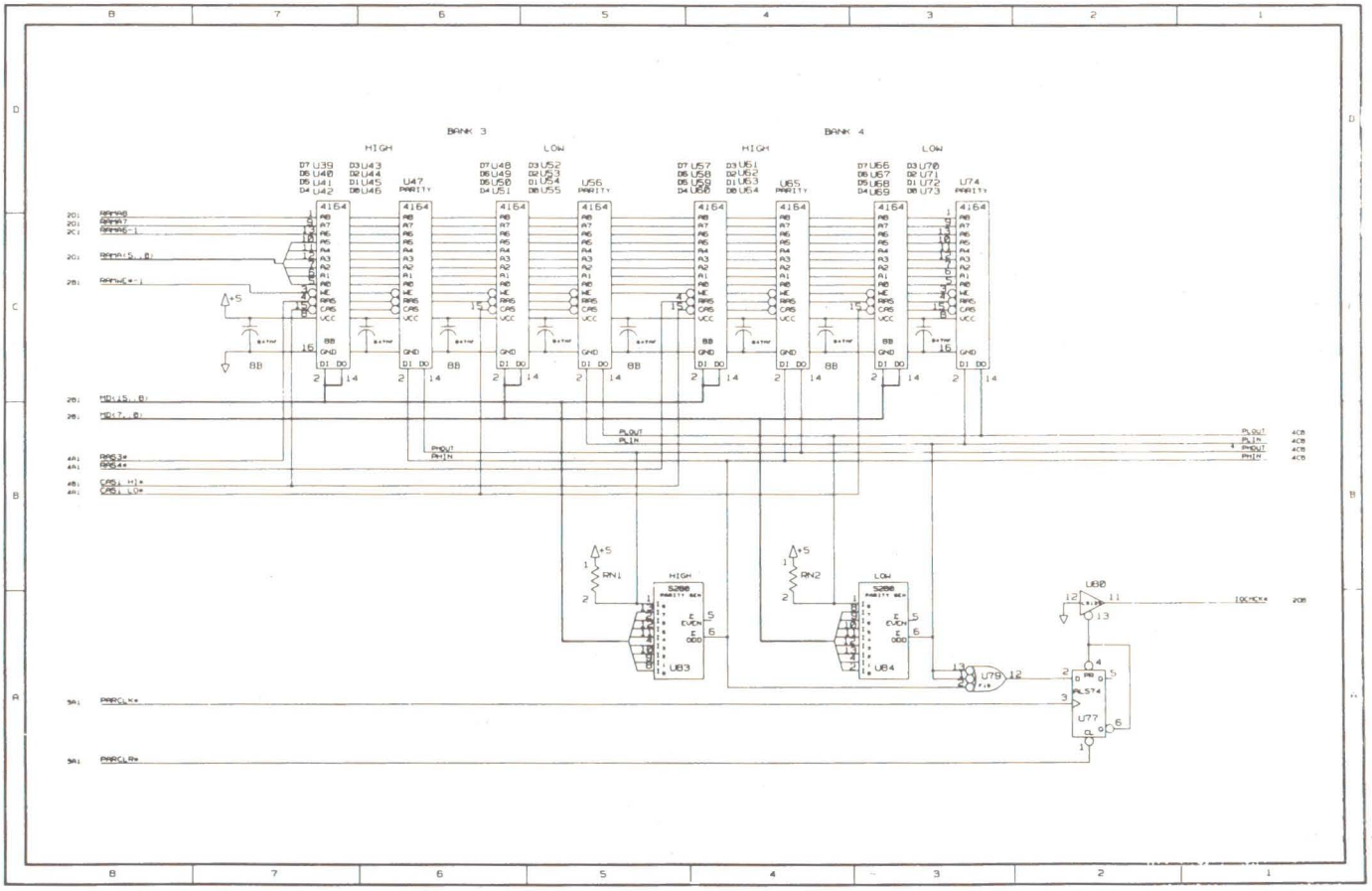
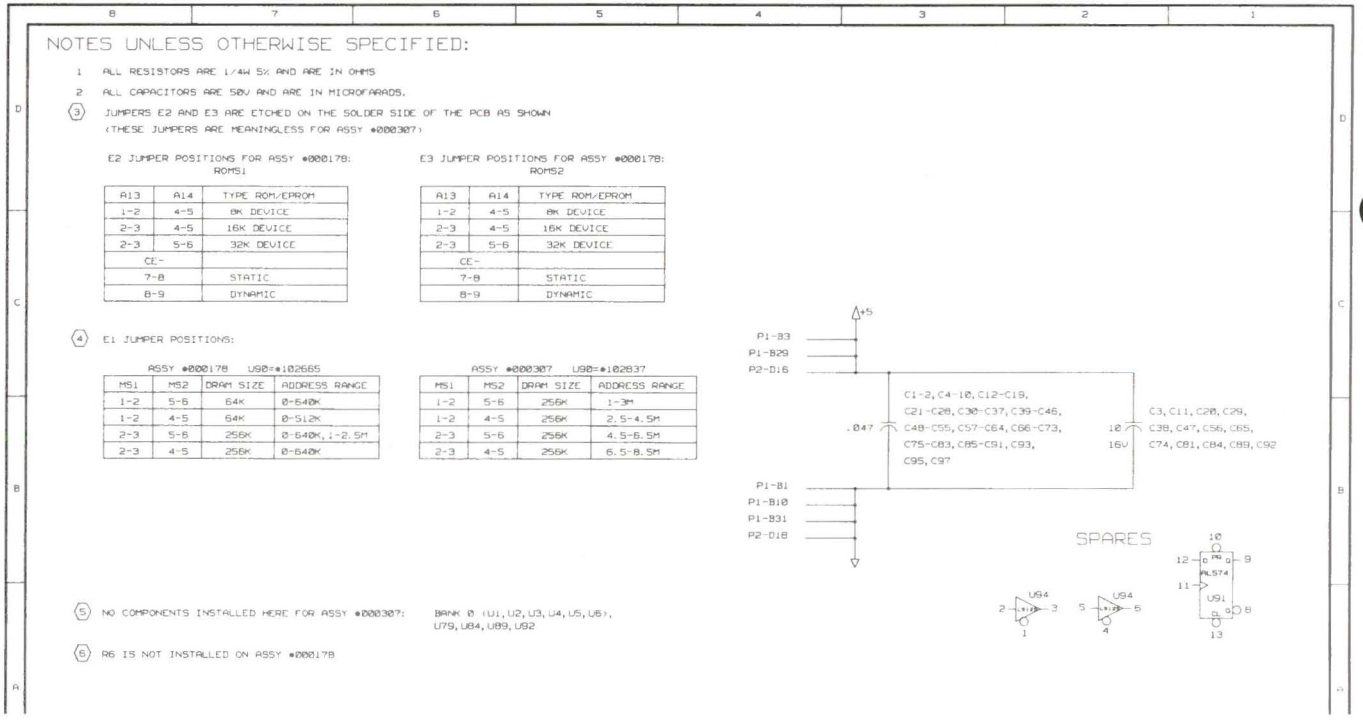


Figure 3-6. COMPAQ DESKPRO 286 System Memory Board Schematics (Page 5 of 5)



NOTES UNLESS OTHERWISE SPECIFIED:

1 ALL RESISTORS ARE 1/4W 5% AND ARE IN OHMS

2 ALL CAPACITORS ARE 50V AND ARE IN MICROFARADS.

(3) JUMPERS E2 AND E3 ARE ETCHED ON THE SOLDER SIDE OF THE PCB AS SHOWN
(THESE JUMPERS ARE MEANINGLESS FOR ASSY #000307)

E2 JUMPER POSITIONS FOR ASSY #000178: ROMS1

A13	A14	TYPE ROM/EPROM
1-2	4-5	8K DEVICE
2-3	4-5	16K DEVICE
2-3	5-6	32K DEVICE
CE-		
7-8		STATIC
8-9		DYNAMIC

E3 JUMPER POSITIONS FOR ASSY #000178: ROMS2

A13	A14	TYPE ROM/EPROM
1-2	4-5	8K DEVICE
2-3	4-5	16K DEVICE
2-3	5-6	32K DEVICE
CE-		
7-8		STATIC
8-9		DYNAMIC

(4) E1 JUMPER POSITIONS:

ASSY #000178 U90=#102665

MS1	MS2	DRAM SIZE	ADDRESS RANGE
1-2	5-6	64K	0-640K
1-2	4-5	64K	0-512K
2-3	5-6	256K	0-640K, 1-2.5M
2-3	4-5	256K	0-640K

ASSY #000307 U90=#102837

MS1	MS2	DRAM SIZE	ADDRESS RANGE
1-2	5-6	256K	1-3M
1-2	4-5	256K	2.5-4.5M
2-3	5-6	256K	4.5-6.5M
2-3	4-5	256K	6.5-8.5M

(5) NO COMPONENTS INSTALLED HERE FOR ASSY #000307: BANK 0 (U1, U2, U3, U4, U5, U6), U79, U84, U89, U92

(6) R6 IS NOT INSTALLED ON ASSY #000178

+5

P1-B3
P1-B29
P2-D16

C1-2, C4-10, C12-C19, C21-C28, C30-C37, C39-C46, C48-C55, C57-C64, C66-C73, C75-C83, C85-C91, C93, C95, C97 — .047

C3, C11, C20, C29, C38, C47, C56, C65, C74, C81, C84, C89, C92 — 10 16V

P1-B1
P1-B10
P1-B31
P2-D18

SPARES

U94 U94 U91 LS74

Figure 3-7. COMPAQ DESKPRO 286 System Memory Board Versions 2 and 3 Schematics (Page 1 of 5)

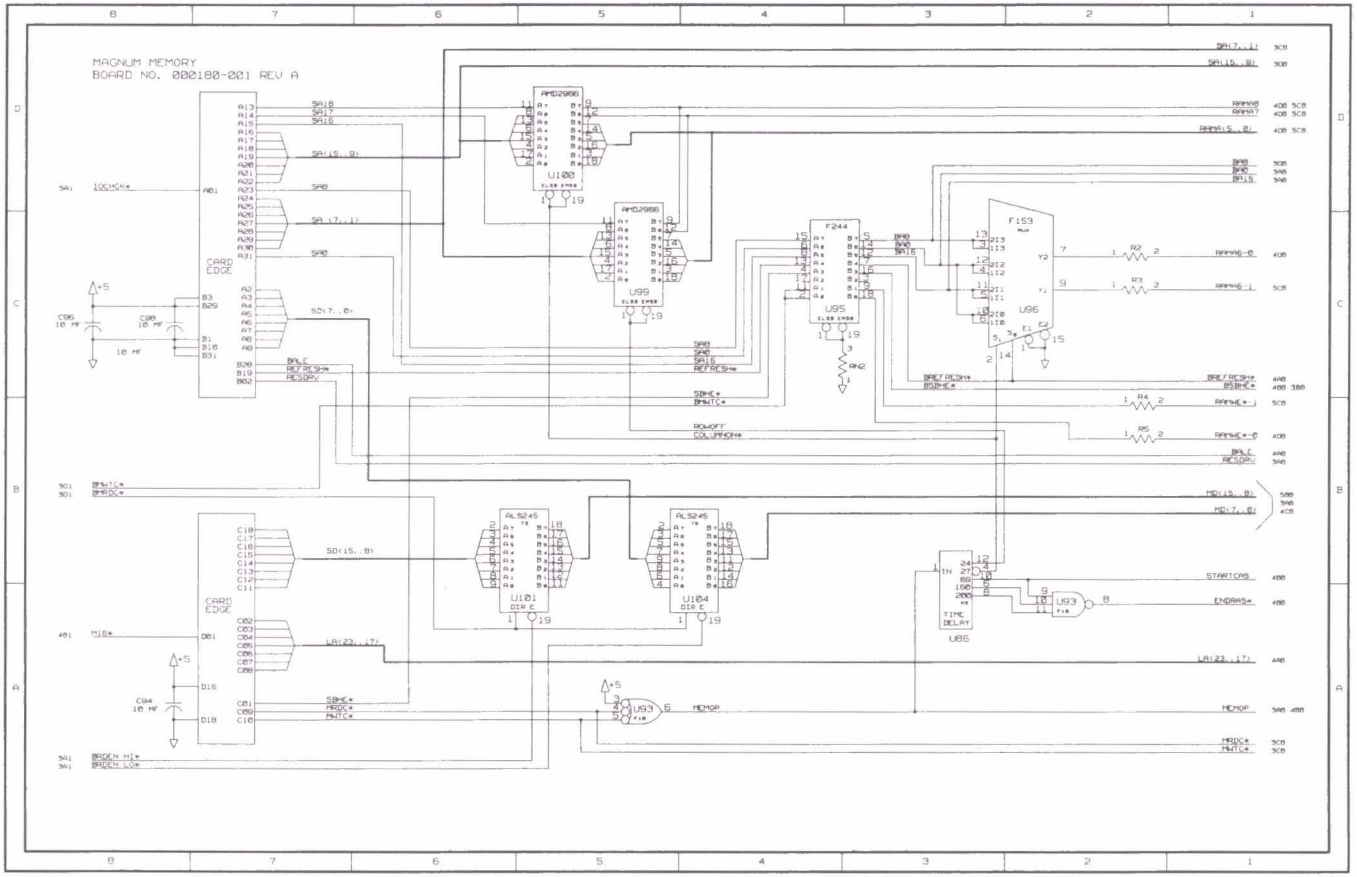


Figure 3-7. COMPAQ DESKPRO 286 System Memory Board Schematics (Page 2 of 5)

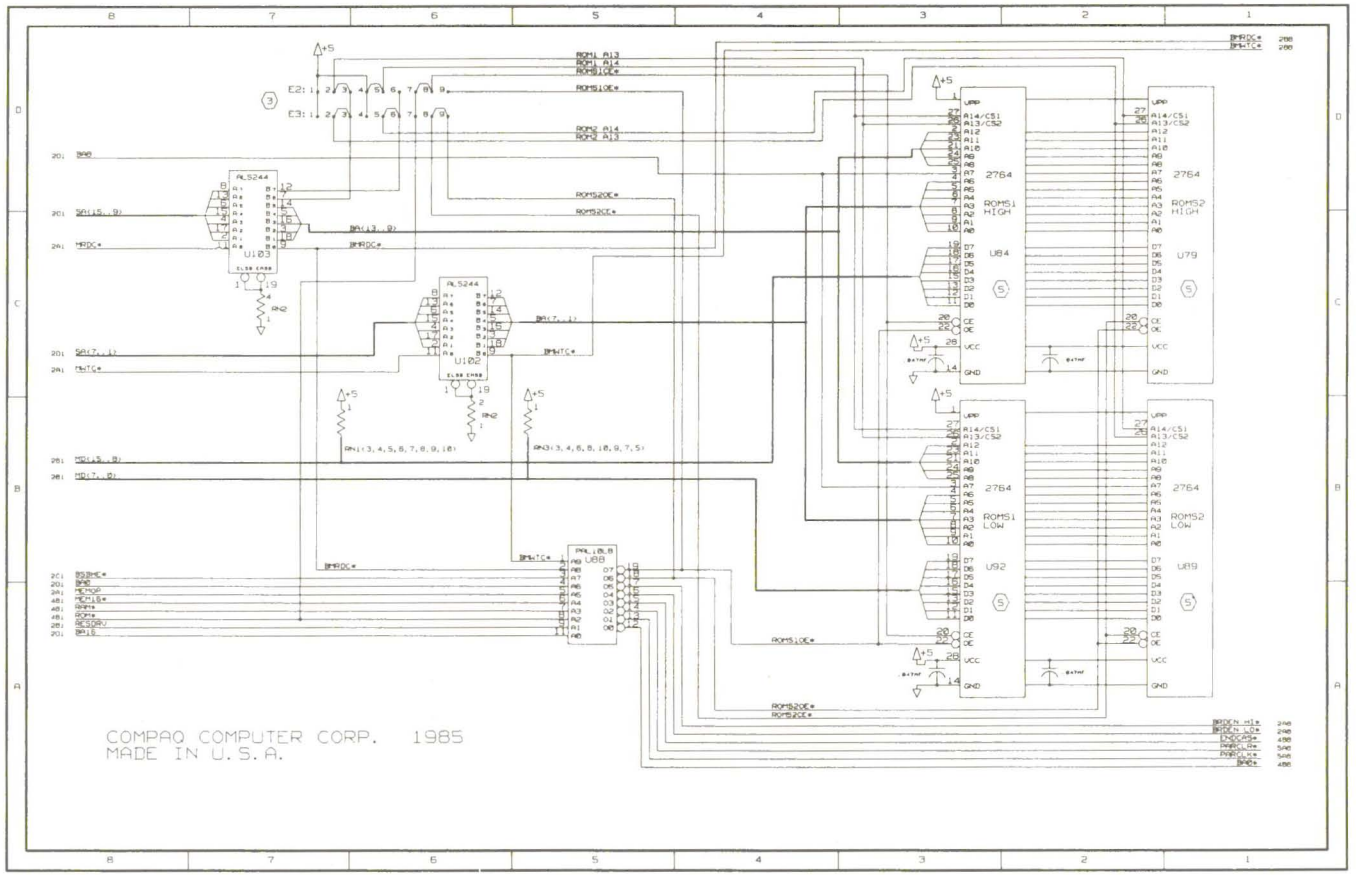


Figure 3-7. COMPAQ DESKPRO 286 System Memory Board Schematics (Page 3 of 5)

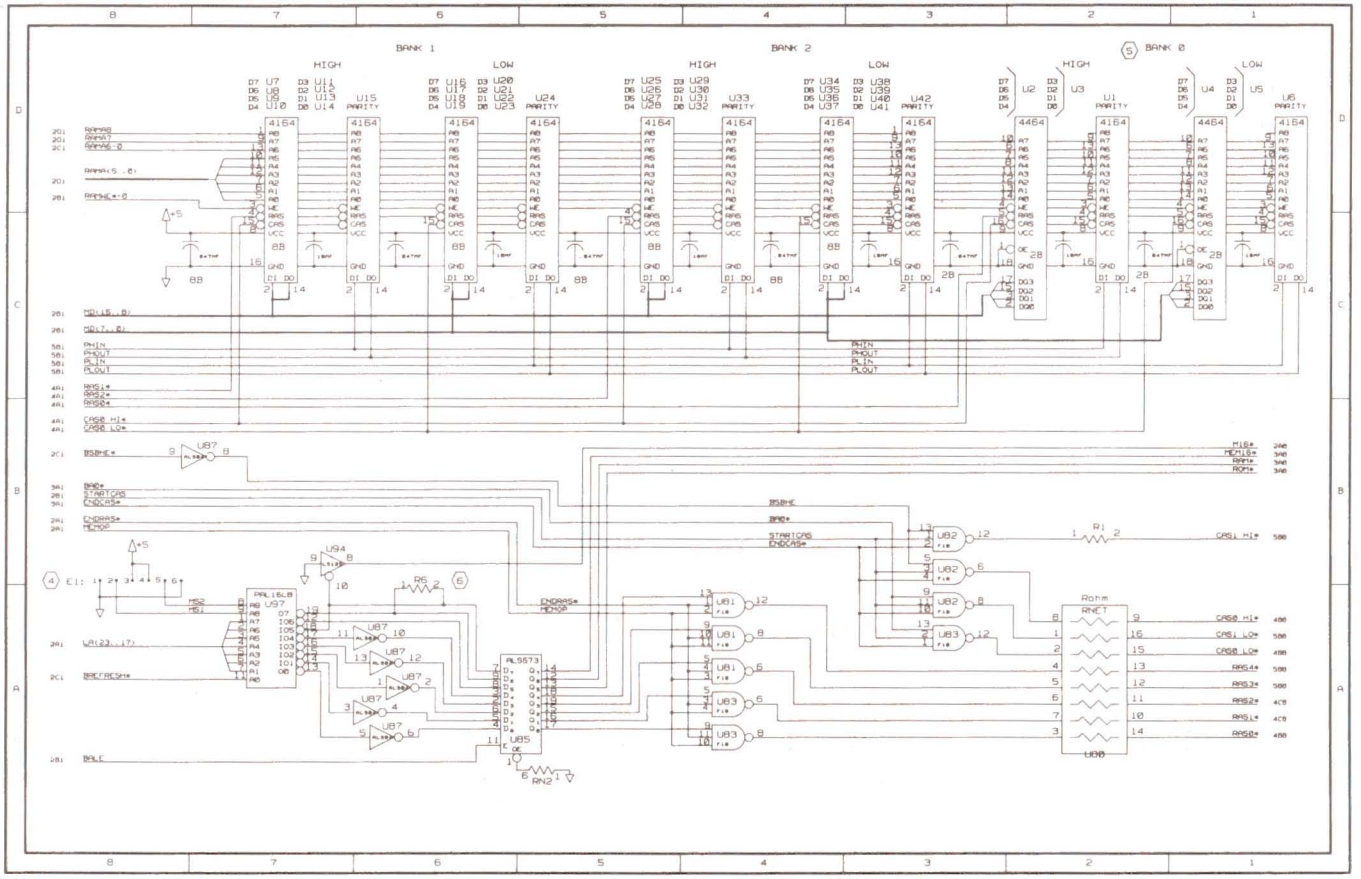


Figure 3-7. COMPAQ DESKPRO 286 System Memory Board Schematics (Page 4 of 5)

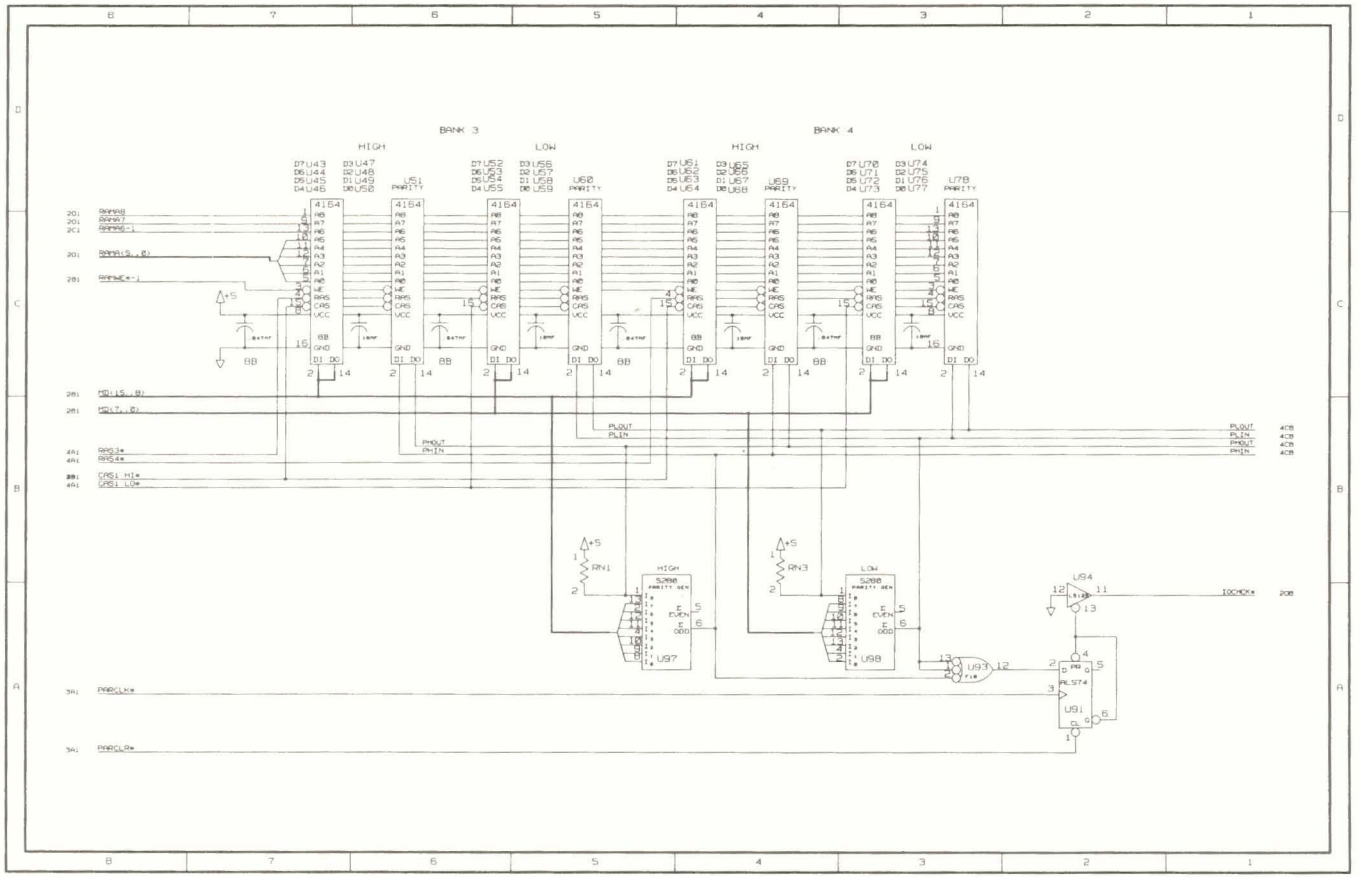


Figure 3-7. COMPAQ DESKPRO 286 System Memory Board Schematics (Page 5 of 5)

Chapter 4
512/2048-KBYTE MEMORY EXPANSION BOARD

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CHAPTER 4
512/2048-KBYTE MEMORY EXPANSION BOARD

Chapter 4
512/2048-KBYTE MEMORY EXPANSION BOARD

4.1 INTRODUCTION

The 512/2048-Kbyte Memory Expansion Board provides for memory expansion of the COMPAQ DESKPRO 286® and the COMPAQ PORTABLE 286® Figures 4-1 and 4-2 show the component layouts for the two versions of the 512/2048-Kbyte Memory Expansion Board. Figure 4-3 shows the functional block diagram.

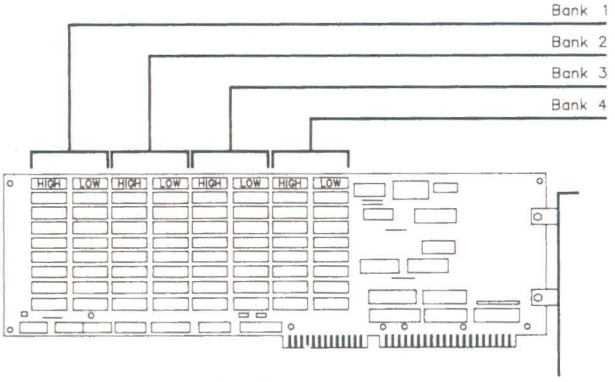

Figure 4-1. 512/2048-Kbyte Memory Expansion Board Version 1 Component Layout

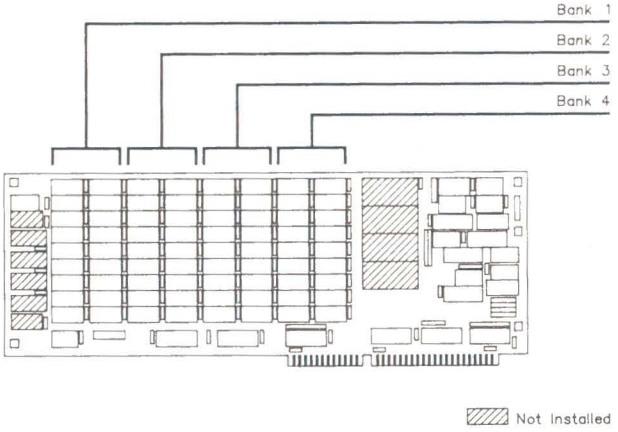

Figure 4-2. 512/2048-Kbyte Memory Expansion Board Version 2 Component Layout

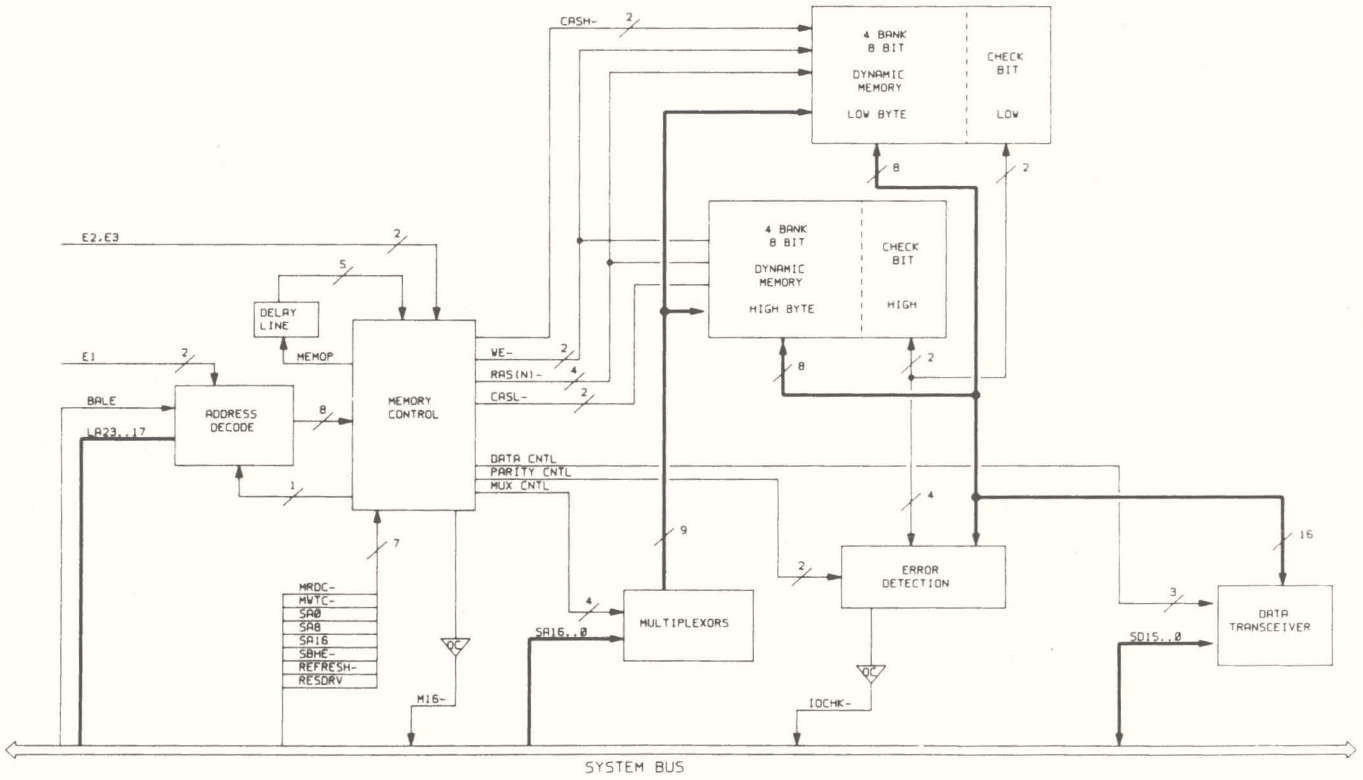

Figure 4-3. 512/2048-Kbyte Memory Expansion Board Functional Block Diagram

4.2 512/2048-KBYTE MEMORY EXPANSION BOARD RAM

The 512/2048-Kbyte Memory Expansion Board has four banks of sockets (Banks 1...4) that provide for system memory expansion using 256K x 1 dynamic RAM (DRAM) chips.

Memory must be installed in full-bank increments (18 DRAMs) in contiguous and ascending order.

There are four possible configurations (address ranges) for the 512/2048-Kbyte Memory Expansion Board:

- 1-3 Megabyte for the COMPAQ PORTABLE 286 and COMPAQ DESKPRO 286 with 640 Kbytes of base memory.
- 5-4.5 Megabyte for the COMPAQ DESKPRO 286 with 2176 Kbytes or the System Memory Board or on the COMPAQ DESKPRO 286 Version 2 System Board. (See Note).
- 5-6.5 Megabytes for the COMPAQ DESKPRO 286 with a 2.5-4.5-megabyte Memory Expansion Board installed.
- 5-8.5 Megabytes for the COMPAQ DESKPRO 286 with a 4.5-6.5-megabyte Memory Expansion Board installed.

NOTE: COMPAQ DESKPRO 286 Version 1 System Board requires the System Memory Board. The Version 2 System Board has the system ROM and RAM on the system board and does not use the System Memory Board.

Tables 4-1 and 4-2 show the possible memory configurations and their corresponding jumper settings.

Table 4-1. Memory Configuration and Corresponding Jumper Settings - Version 1 Memory Expansion Board

Jumper Setting	Address Range	Bank 1	Bank 2	Bank 3	Bank 4
E1-E2, E5-E6	1-3 MB	512 KB	512 KB	512 KB	512 KB
E1-E2, E4-E5	2.5-4.5 MB	512 KB	512 KB	512 KB	512 KB
E2-E3 E5-E6	4.5-6.5 MB	512 KB	512 KB	512 KB	512 KB
E2-E3 E4-E5	6.5-8.5 MB	512 KB	512 KB	512 KB	512 KB

Note: Use the instructions that come with the COMPAQ memory option kit to properly configure your memory expansion board.

Table 4-2. Memory Configuration and Corresponding Jumper Settings - Version 2 Memory Expansion Board

E1 Jumper Setting	Address Range	Bank 1	Bank 2	Bank 3	Bank 4
1-2,5-6	1-3 MB	512 KB	512 KB	512 KB	512 KB
1-2,4-5	2.5-4.5-MB	512 KB	512 KB	512 KB	512 KB
2-3,5-6	4.5-6.5 MB	512 KB	512 KB	512 KB	512 KB
2-3,4-5	6.5-8.5 MB	512 KB	512 KB	512 KB	512 KB

Note: Use the instructions that come with the COMPAQ memory option kit to properly configure your memory expansion board.

The 512/2048-Kbyte Memory Expansion Board uses approved 256K x 1 DRAM chips with a response time of 150 ns or faster. (CAS access time must be 75 ns or faster.) Use Only 256K x 1 DRAM in the 512/2048-Kbyte Memory Expansion Board.

Never add a memory expansion board with an address range that will overlap with any existing memory boards. Be sure to install memory expansion boards so that memory is contiguous through the specified address range for a particular memory expansion board, all four banks of RAM must be installed.

NOTE: Use the instructions that come with the COMPAQ Memory Expansion Board Option Kit to properly configure your memory board.

The schematics supplied in Chapter 3, COMPAQ DESKPRO System Memory Board are generally accurate for the board except that memory bank 0 and ROMs are not installed.

Figure 4-4 shows the relationship between the memory map and the installed RAM banks for each configuration.

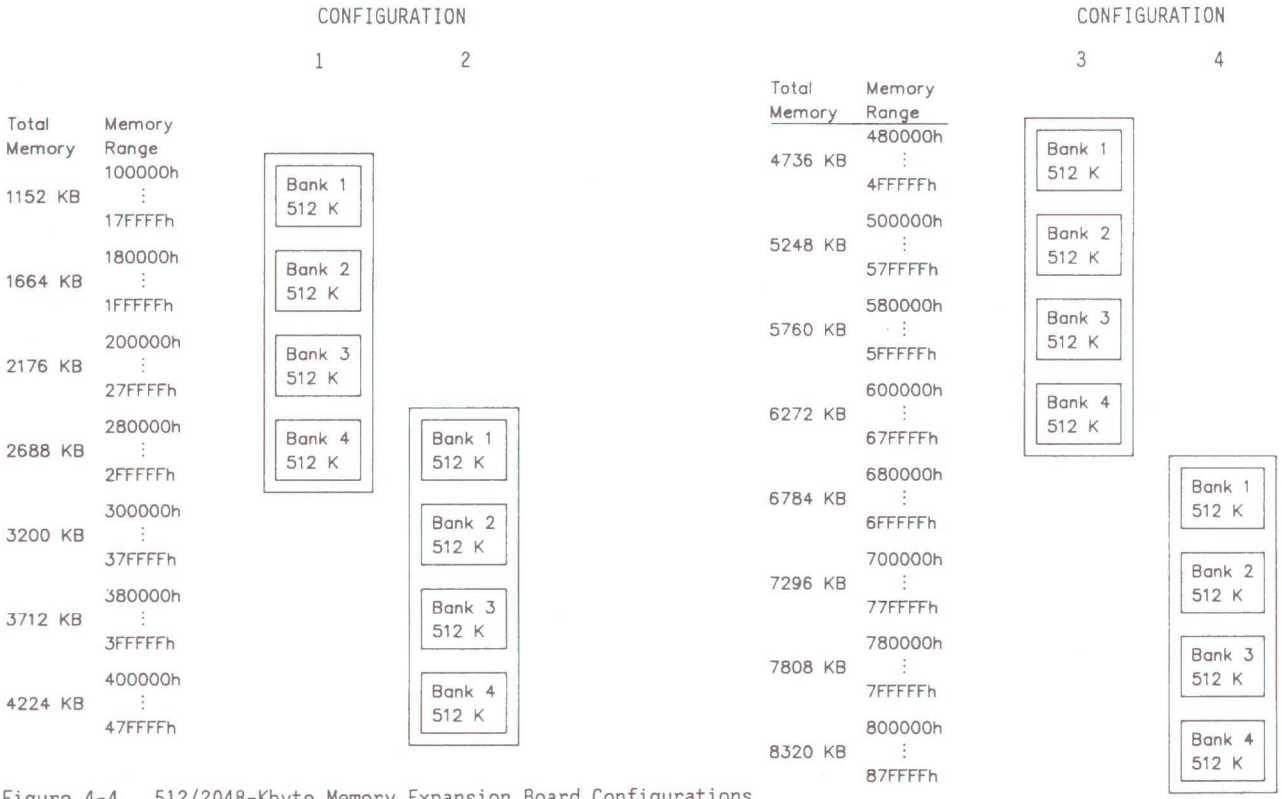

Figure 4-4. 512/2048-Kbyte Memory Expansion Board Configurations

Chapter 5

MULTIPURPOSE CONTROLLER BOARDS

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CHAPTER 5
MULTIPURPOSE CONTROLLER BOARDS

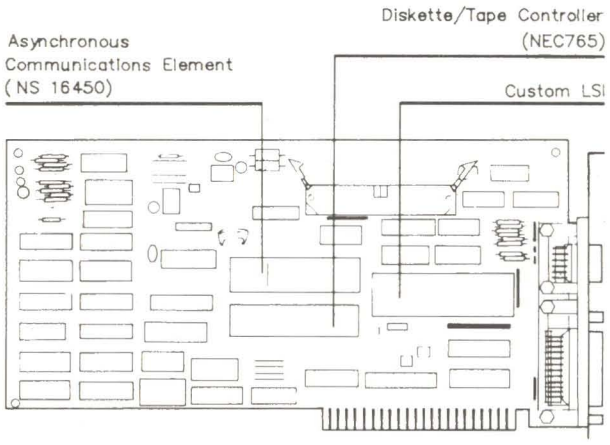


Figure 5-1. Multipurpose Controller Board Component Layout

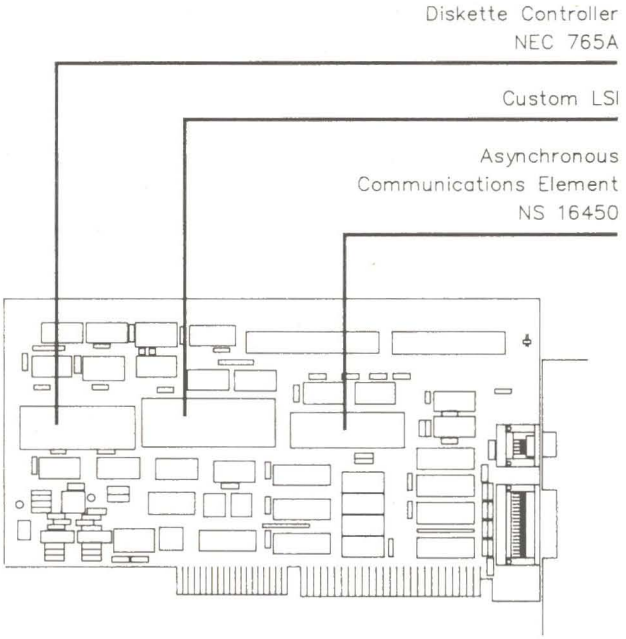


Figure 5-2. Multipurpose Fixed Disk Controller Board Componet Layout

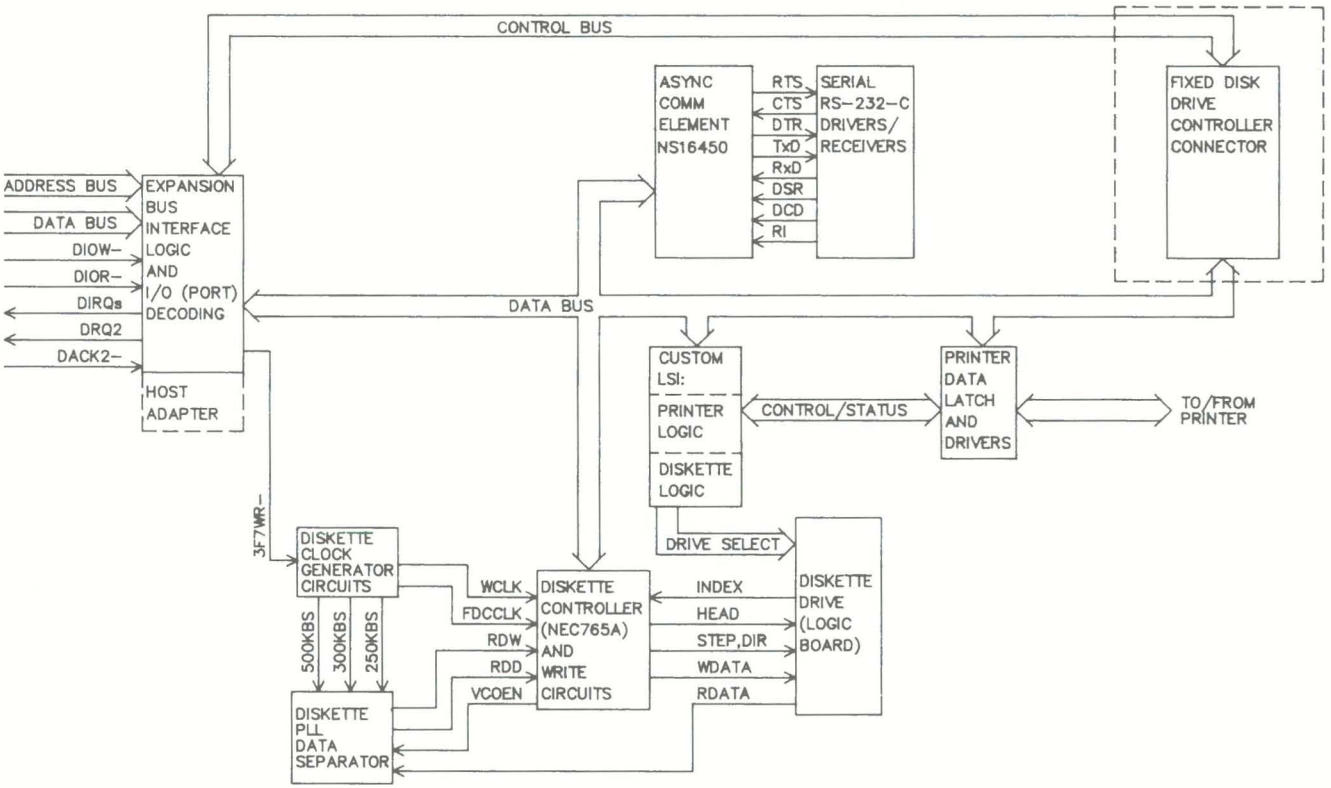


Figure 5-3. Functional Block Diagram for Both Multipurpose Controller Boards.

Chapter 5
MULTIPURPOSE CONTROLLER BOARDS

5.1 INTRODUCTION

The multipurpose controller and multipurpose fixed disk controller boards are described in this chapter. The multipurpose controller board is used in both the COMPAQ DESKPRO 286® and COMPAQ PORTABLE 286® Personal Computers, which operate at 8 and 6 MHz.

The multipurpose fixed disk controller board is used in COMPAQ DESKPRO 286 Personal Computer, which operates at 12 MHz.

Both controller boards supply the diskette drive and fixed disk drive backup controller board functions, as well as asynchronous and parallel printer communications functions. In addition to the above functions, the multipurpose fixed disk controller board also interfaces with a 40-megabyte fixed disk drive.

To interface with the multipurpose fixed disk controller board, the 40-megabyte fixed disk drive has an integrated controller on a logic board that is attached to the drive. The multipurpose fixed disk controller circuitry provides address decoding, buffers, and a control and data connector for the fixed disk drive controller.

NOTE: If a second 40-megabyte fixed disk drive is added to a COMPAQ DESKPRO 286, a 40-megabyte fixed disk drive back-up cannot be added to the system's configuration.

Figure 5-1 show the component layout for the multipurpose controller board. Figure 5-2 shows the component layout for the multipurpose fixed disk controller board.

Figure 5-3 shows the functional block diagram for both multipurpose controller boards.

Three functions of both controller boards are controlled by programmable devices:

- Diskette and fixed disk drive backup controller functions are handled by an NEC765A floppy Disk controller device.
- Asynchronous communications are handled by a National Semiconductor NS16450.
- Parallel printer output and status are handled by a custom large-scale-integrated (LSI) device. This device also controls some drive control functions.

The following sections describe these programmable devices and other functions of the multipurpose controller boards.

Table 5-1 lists the I/O ports used on the multipurpose controller boards.

5.2 DRIVE CONTROLLER CIRCUITS

The drive controller board circuits control one or two 1.2-MB or 360-KB diskette drives and one fixed disk drive backup (10 or 40-MB).

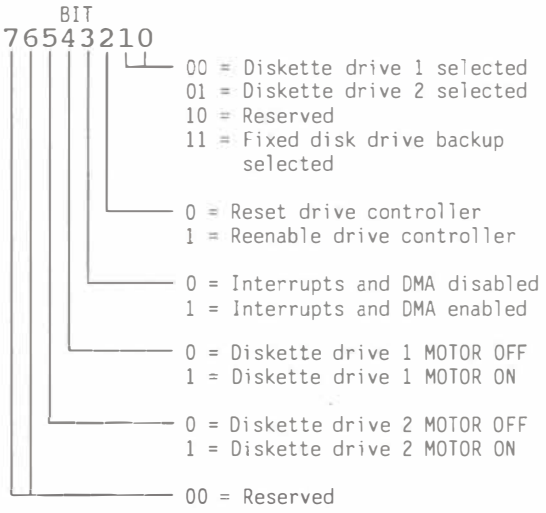
The drive controller uses four I/O port addresses to transmit data to and from a diskette drive or fixed disk drive backup, to control the drive functions, and to read the current drive status. Table 5-2 lists the port addresses for the drive controller.

Table 5-2. Drive Controller Port Addresses

Port 1	Port 2	R/W	Register Function
3F2h	372h	W	Drive Control
3F4h	374h	R	Drive Status
3F5h	375h	R/W	Data
3F7h	377h	W	Data Transfer Rate Control
3F7h	377h	R	Diskette and Fixed Disk Status

DRIVE CONTROL (3F2h, WRITE ONLY)

The Drive Control register is part of the Custom LSI device. It controls functions such as Interrupt and DMA Enable, Drive MOTOR ON, DRIVE SELECT, and Controller Reset. The format for this register is as follows:



MAIN STATUS (3F4h, READ-ONLY)

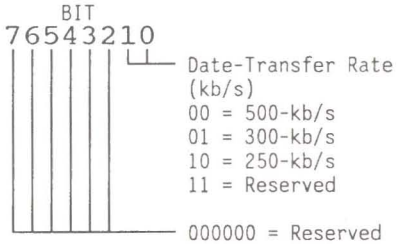
The Main Status register is part of the NEC765A drive controller. It is used as the Diskette Status register.

DATA (3F5h)

The Data register is part of the NEC765A drive controller. Data and NEC765A controller commands are written, and data and status bytes are read from the controller through this port.

DATA TRANSFER RATE CONTROL (3F7h, WRITE-ONLY)

The DATA-TRANSFER RATE CONTROL register shares port 3F7h with the DISKETTE1 AND FIXED DISK1 STATUS register. This register contains the current data-transfer rate in kilobits per second (kb/s). The format for this register is:



DISKETTE1 AND FIXED DISK1 STATUS (3F7h, READ ONLY)

This register provides both diskette1 status information (bit <7>) and fixed disk1 status information (bits <6...0>). The format for this register is as follows:

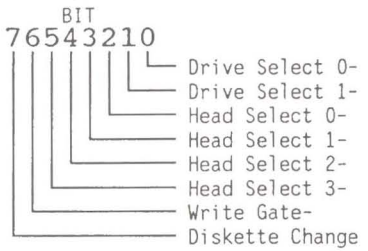


Table 5-1. Controller Board I/O Ports

Port	R/W	Register Functions	Multipurpose Controller Board	Multipurpose Fixed Disk Controller Board
2F8h	R/W	COM2 Divisor Latch LSB (with DLA bit = 1 (Note 1))	(J2,2-3),(J4,2-3)	(J1, Pos. 2)
2F8h	R	COM2 Received Data (with DLA bit = 0 (Note 1))	"	"
2F8h	W	COM2 Transmit Data (with DLA bit = 0 (Note 1))	"	"
2F9h	R/W	COM2 Divisor Latch MSB (with DLA bit = 1 (Note 1))	"	"
2F9h	R/W	COM2 Interrupt Enable (with DLA bit = 0 (Note 1))	"	"
2FAh	R	COM2 Interrupt ID	"	"
2FAh	W	COM2 Reserved	"	"
2FBh	R/W	COM2 Line Control	"	"
2FCh	R/W	COM2 Modem Control	"	"
2FDh	R	COM2 Line Status	"	"
2FEh	R	COM2 Modem Status	"	"
2FFh	R/W	COM2 Reserved	"	"
370h	R/W	Diskette2 Reserved (Note 2)	(J1,1-2)	(J2, Pos. 2)
371h	R/W	Diskette2 Reserved (Note 2)	"	"
372h	W	Diskette2 Drive Control (Note 2)	"	"
372h	R	Diskette2 Reserved (Note 2)	"	"
373h	R/W	Diskette2 Reserved (Note 2)	"	"
374h	R	Diskette2 Main Status (Note 2)	"	"
374h	W	Diskette2 Reserved (Note 2)	"	"
375h	R/W	Diskette2 Data (Note 2)	"	(J1, Pos. 2)
377h	R	Diskette2 and Fixed Disk 2 Status (Note 2)	"	"
377h	W	Diskette2 Data Rate (Note 2)	"	"
3BCh	R/W	Printer1 Data	(J3,2-3)	SW2 ON
3BDh	R	Printer1 Status	"	"
3BDh	W	Printer1 Reserved	"	"

Notes:
1. The DLA bit is in the Line Control register. This bit must be set (=1) to access the divisor latches and reset (=0) to access the Data and the Interrupt Enable registers.
2. Diskette1 and Diskette2 are referencing the capabilities of using two addressable diskette controller boards, not diskette drives.

(Continued)

Table 5-1. (Continued)

Port	R/W	Register Functions	Multipurpose Controller Board	Multipurpose Fixed Disk Controller Board
3BEh	R/W	Printer1 Control	(J2,2-3)	SW2 ON
3BFh	R/W	Printer1 Reserved	"	"
3F0h	R/W	Diskette1 Reserved	(J1,2-3)	(J2, Pos. 1)
3F1h	R/W	Diskette1 Reserved	"	"
3F2h	W	Diskette1 Drive Control	"	"
3F2h	R	Diskette1 Reserved	"	"
3F3h	R/W	Diskette1 Reserved	"	"
3F4h	R	Diskette1 Main Status	"	"
3F4h	W	Diskette1 Reserved	"	"
3F5h	R/W	Diskette1 Data	"	"
3F7h	R	Diskette1 and Fixed Disk 1 Status (Note 1)	"	"
3F7h	W	Diskette1 Data Rate	"	"
3F8h	R/W	Divisor Latch LSB (with DLA bit = 1 (Note 2))	(J2,1-2),(J4,1-2)	(J1 Pos. 1)
3F8h	R	COM1 Received Data (with DLA bit = 0 (Note 2))	"	"
3F8h	W	COM1 Transmit Data (with DLA bit = 0 (Note 2))	"	"
3F9h	R/W	COM1 Divisor Latch MSB (with DLA bit = 1 (Note 2))	"	"
3F9h	R/W	COM1 Interrupt Enable (with DLA bit = 0 (Note 2))	"	"
3FAh	R	COM1 Interrupt ID	"	"
3FAh	W	COM1 Reserved	"	"
3FBh	R/W	COM1 Line Control	"	"
3FCh	R/W	COM1 Modem Control	"	"
3FDh	R	COM1 Line Status	"	"
3FEh	R	COM1 Modem Status	"	"
3FFh	R/W	COM1 Reserved	"	"

Notes:
1. Only bit D7 of this port address is resident on the multipurpose controller board. Bits D<6..0> are resident on the fixed disk drive controller board.
2. The DLA bit is in the Line Control Register. This bit must be set (=1) to access the divisor latches and reset (=0) to access the Data and the Interrupt Enable registers.

Drive Controller (NEC765A)

The NEC765A Floppy Disk Controller is the heart of the multipurpose controller boards. It accepts commands from the system and controls most drive functions and the transfer of data to the drives.

The NEC765A operates in the DMA mode for data transfers to the system. It issues a DMA request signal (DRQ2) and receives a DMA Acknowledge signal (DACK2-) for each byte transferred.

The NEC765A has two registers, a Data register and the Main Status register (See Table 5-3). The Data register is used to program the device or to transmit or receive blocks of data.

Table 5-3. NEC765A Registers

Port		
1	2	Function
3F4h	374h	Main Status Register
3F5h	375h	Data Register

All NEC765A commands have three operating phases:

- The command phase, where the NEC765A receives the command from the system.
- The execution phase, where the NEC765A carries out the command.
- The results phase, where the status and results are read back from the NEC765A to the system.

For detailed command information, refer to the NEC765A or Intel 8272A component data sheets.

The Custom LSI Device

The Custom LSI device is a circuit for address decoding and control signal timing. It is addressed as a port device to control the diskette drive motors and for drive selection.

Programmable Data Transfer Rate

The system can transfer data with the diskette drives at 250-, 300-, or 500-kb/s. Table 5-4 lists the data transfer rates used by various drives. The Data-Transfer Rate Control register format describes the byte that specifies the present transfer rate.

Table 5-4. Programmable Data Transfer Rate

Transfer Rate	When Used
500 kb/s	1.2-Megabyte Diskette Drive with 1.2-Megabyte media
500 kb/s	40-Megabyte Fixed Disk Drive Backup with 40-Megabyte media
300 kb/s	1.2-Megabyte Diskette Drive with 360-kilobyte media
250 kb/s	Double-density Diskette Drive or Fixed Disk Drive Backup with 10-Megabyte media

Data Separator

Data separation is a process of separating the Data and Clock signal from the drives into separate Clock and Data lines. Several devices form a voltage-controlled oscillator/phase-locked loop circuit to perform the data separation.

Write Precompensation and Write Control

Write precompensation is a process of time shifting write data bits to help negate an opposite shift induced during magnetic recording. This process increases the data integrity at high data densities. The data density increases as the diskette drive head approaches the center tracks (track 40 or 80).

Write precompensation is always on. The amount of precompensation varies with the data transfer rate (See Table 5-5).

Table 5-5. Write Precompensation Amounts

Transfer Rate	Precompensation
500-kilobytes per second	125 ns
300-kilobytes per second	208 ns
250-kilobytes per second	250 ns

5.3 ASYNCHRONOUS COMMUNICATIONS CIRCUITS

The asynchronous serial port is always enabled, except on revision level G (or later) multipurpose controller boards or multipurpose fixed disk controller board, which can disable the port by setting Switch 3 in switch bank SW1 to the OFF position.

The heart of the asynchronous communication circuit is a National Semiconductor NS16450 Asynchronous Communications Element (ACE). This device converts data received in a parallel format from the system to data in a serial format for a serial printer or other serial device. It also performs the reverse function by converting the serial data to parallel.

This device is I/O-mapped at ports 3F8h..3FFh or 2F8h..2FFh, depending on whether COM1 or COM2 is selected (see Table 5-6).

Table 5-6. I/O Ports for Asynchronous Communications

Port 1	Port 2	Function
3F8h	2F8h	Receiver Buffer (when read by system), Transmitter Holding Register (when written to by system) or
See Note		Baud Rate Divisor Latch
3F9h	2F9h	Interrupt Enable or
See Note		Baud Rate Divisor Latch
3FAh	2FAh	Interrupt ID (read only)
3FBh	2FBh	Line Control
3FCh	2FCh	Modem Control
3FDh	2FDh	Line Status
3FEh	2FEh	Modem Status
3FFh	2FFh	Scratch

Note: When bit 7 of the Line Control Register (LCR) is set (=1), writing to the first two ports programs the divisor rate for the Baud Rate Generator.

ACE RECEIVER BUFFER OR TRANSMITTER HOLDING REGISTER (3F8h)

This register contains the byte just received or the next byte to be transmitted by the ACE.

ACE BAUD RATE DIVISOR LATCH (3F8h, 3F9h)

The NS16450 contains a built-in baud rate generator that divides the input clock (1.8432 MHz) by a divisor to create a desired baud rate or serial transmission frequency.

The divisor is found according to the formula:

Divisor = 1843200 / (Desired Baud Rate x 16)

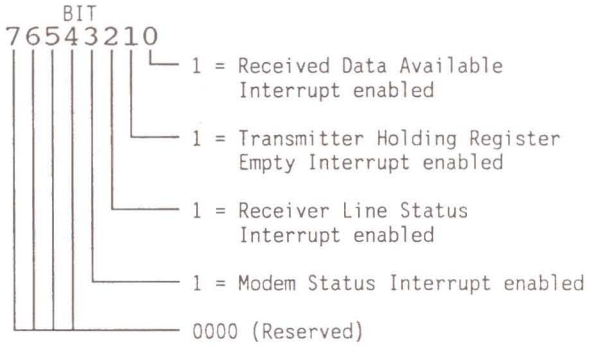
The following tabulation gives the divisors calculated for specific baud rates:

Baud Rate	Divisor
110	1047
150	768
300	384
600	192
1200	96
2400	48
4800	24
9600	12

Setting bit <7> (=1) enables the first two I/O addresses of the Line Control register as the addresses for the least- and most-significant bytes of the 16-bit baud rate divisor.

ACE INTERRUPT ENABLE REGISTER (3F9h)

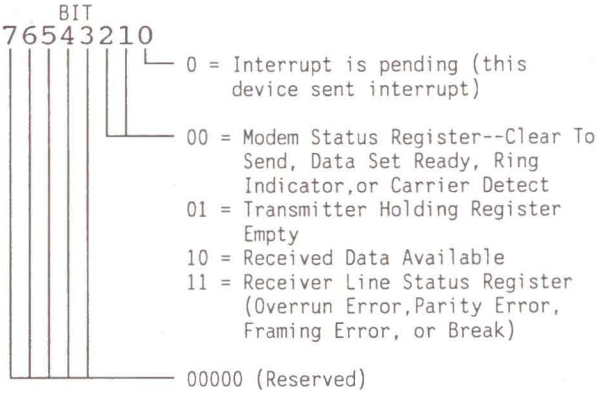
The bits of this register enable up to four interrupt sources.



ACE INTERRUPT ID REGISTER (3FAh, READ-ONLY)

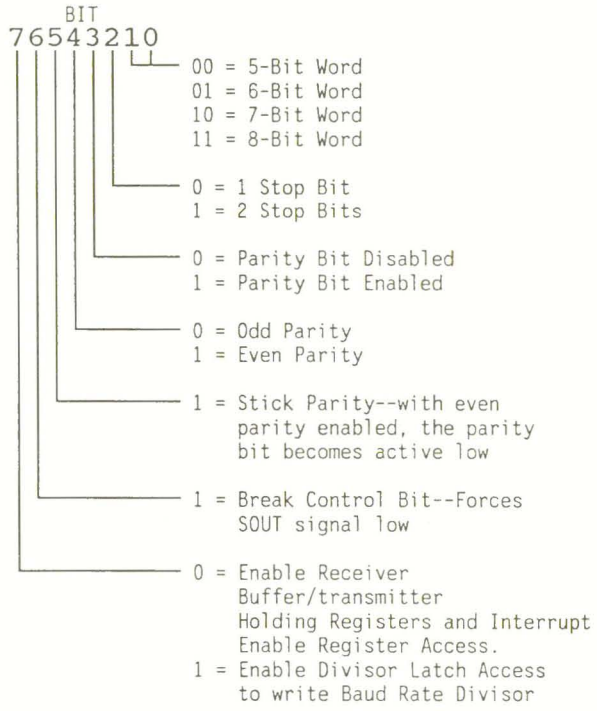
When a hardware interrupt occurs, the system searches for the device sending the interrupt and the reason for that interrupt.

This register contains a bit that flags the ACE as the source of the interrupt and two bits that specify the reason for the interrupt. The ACE interrupts are prioritized, and listed below with the lowest-priority interrupt first. To clear the interrupt, read the contents of the register shown.



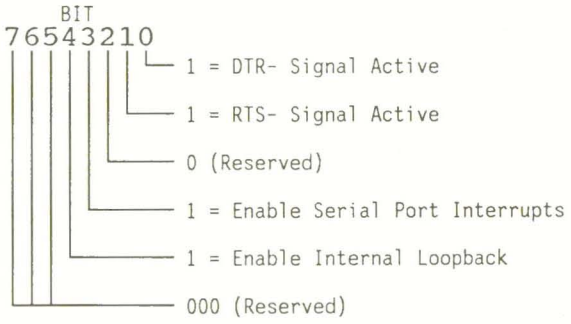
ACE LINE CONTROL REGISTER (3FBh)

This register specifies the serial data transmission format.



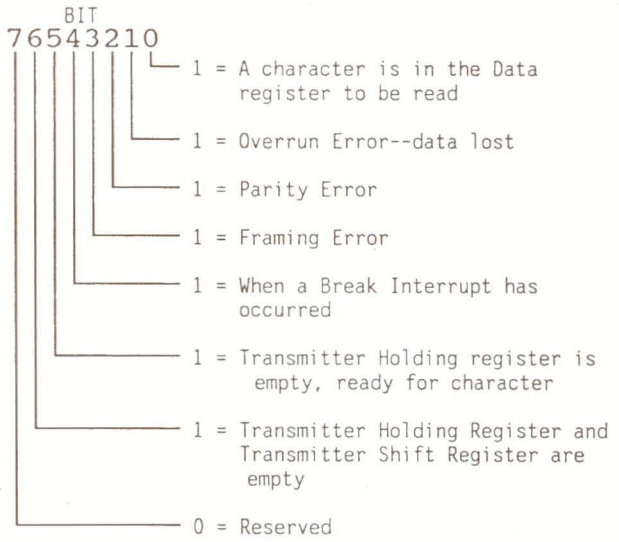
ACE MODEM CONTROL REGISTER (3FCh)

This register controls the modem interface lines.



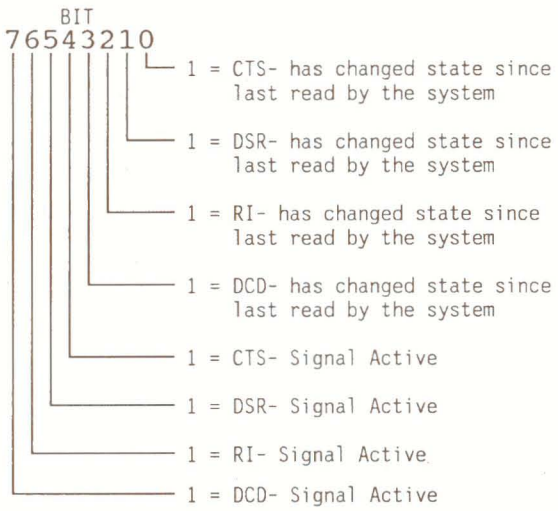
ACE LINE STATUS REGISTER (3FDh, READ-ONLY)

This register contains the status of the current data transfer.



ACE MODEM STATUS REGISTER (3FEh, READ-ONLY)

This register contains the status of the modem interface lines.



ACE RESERVED (3FFh)

This is not currently used.

5.4 PRINTER CIRCUITS

The printer port is enabled either by setting Jumper J3, Pins 2-3, on the multipurpose controller board or by setting Switch 2 in switch bank SW1, on the multipurpose fixed disk controller board. When the printer is disabled, the printer port of a different controller can be used instead of the multipurpose controller board or multipurpose fixed disk controller board port.

The printer circuits are addressed as ports. Data is sent in parallel to the printer, and printer status is received from the printer through these ports.

Before printing, the system must select the printer for output (through the Printer Control register). For each byte sent to the printer, the system:

1. Checks the Printer Status register.
   If the busy, paper out, or printer fault signals are active, the system either waits until the status changes or it shows an error message.
2. Sends a byte of data to the Printer Data register, then pulses the printer STROBE signal (through the Printer Control Register) for 500 ns (or longer).
3. Monitors the Printer Status register for acknowledgement of the data byte before sending the next byte.

In addition to data lines to the printer, the system also has several control lines that control printer functions.

Printer functions are controlled by writing to or reading from I/O ports. Table 5-7 provides I/O Ports for Printer Access.

Table 5-7. I/O Ports For Printer Access

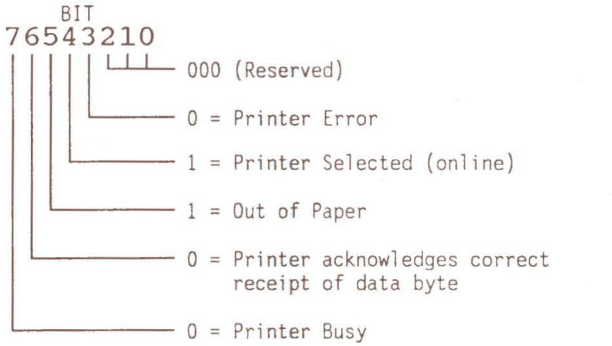
Port	R/W	Function
3BCh	R/W	Printer Data register
3BDh	R	Printer Status register
3BEh	R/W	Printer Control register

PRINTER DATA REGISTER (3BCh)

Each byte written to the Printer Data register (read or write) is latched into a loopback register and is sent to the printer. The register contents can be read back (for test purposes).

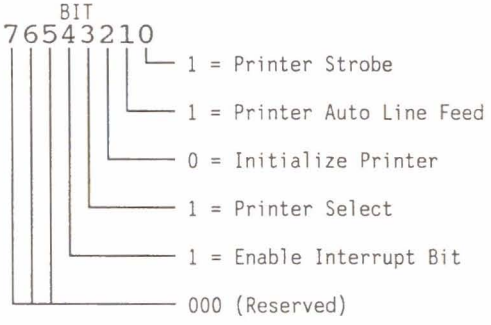
PRINTER STATUS REGISTER (3BDh, READ-ONLY)

This register contains the current printer status.



PRINTER CONTROL REGISTER (3BEh)

This register selects the printer for output, strobes the data into the printer, and performs other printer control functions.



5.5 JUMPERS

Jumpers for both the multipurpose controller board and the multipurpose fixed disk controller board are given in this section.

Multipurpose Controller Board Jumpers

The multipurpose controller board has four jumpers which are described in Table 5-8. The jumper locations are shown in Figure 5-4.

Table 5-8. Multipurpose Controller Board Jumpers

Jumper	Function
J1	Diskette Controller Board Base-Address Select. This address-selection option is available for special applications and under normal circumstances should not be changed. (J1,1-2) Secondary (Diskette2) Address Select (370h) (J1,2-3) Primary (Diskette1) Address Select (3F0h, standard) "Diskette1 and Diskette2" are referencing the capabilities of using two addressable diskette controller boards, not diskette drives.
J2	Asynchronous Communications Port Base-Address Select. This address-selection option allows two asynchronous communication ports to operate at the same time, using two I/O port ranges. Jumpers J2 and J4 are generally set together (see jumper J4). (J2,1-2) Asynchronous communications Port 1 (COM1) selected (3F8h, standard) (J2,2-3) Asynchronous communications Port 2 (COM2) selected (2F8h)

(Continued)

Table 5-8. (Continued)

Jumper	Function
J3	Printer Enable. This jumper allows the printer port decoding to be disabled. This option prevents conflicts with I/O addresses 3BCh-3BFh when a multifunction board is installed that has Printer1 I/O port decoding. (J3,1-2) Parallel Printer Port disabled (J3,2-3) Parallel Printer Port enabled (standard)
J4	Asynchronous Communications Port Interrupt Select. This jumper option allows the interrupt request line associated with the asynchronous communications port to be changed when the selected asynchronous communications port is changed. COM1 and IRQ4 are used together, as are COM2 and IRQ3. (J4,1-2) Asynchronous Communications Port IRQ4 (COM1) selected (standard) (J4,2-3) Asynchronous Communications Port IRQ3 (COM2) selected

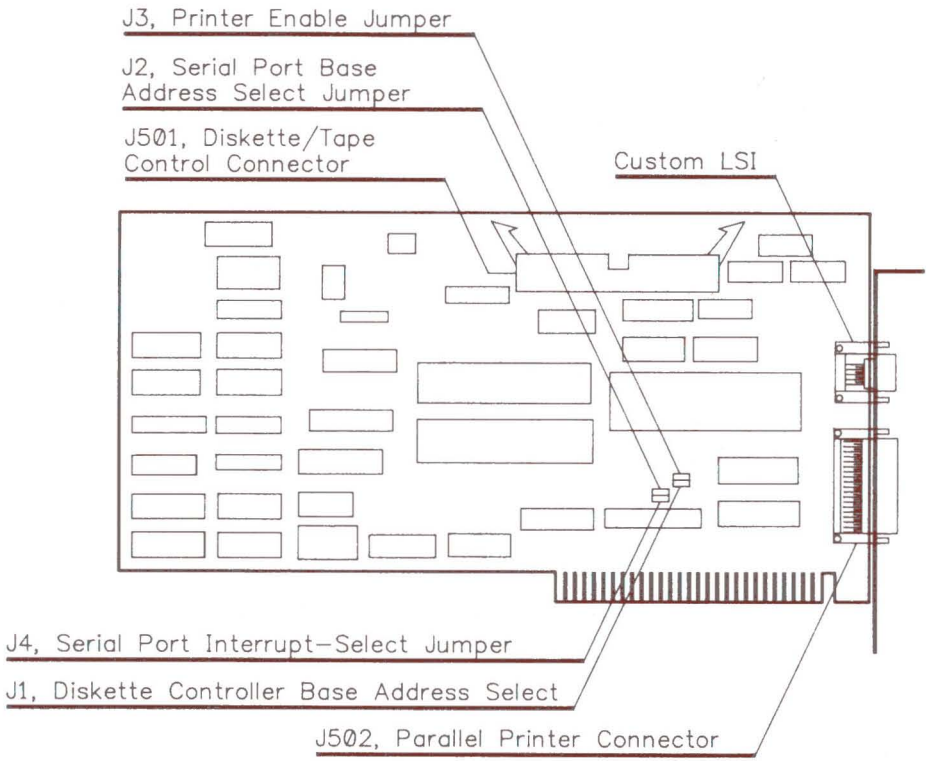


Figure 5-4. Multipurpose Controller Board Jumper Locations

Multipurpose Fixed Disk Controller Board Jumpers

The multipurpose fixed disk controller board jumpers are described in Table 5-9 and are shown in Figure 5-5.

Table 5-9. Multipurpose Fixed Disk Controller Board Jumpers

Jumper	Function
J1	Asynchronous Communications Port Base-Address and Interrupt Request Select. This address-selection option allows two asynchronous communications ports to operate at the same time, using two I/O port ranges. Position 1, Com1-Asynchronous Communications Port 1 selected (3F8H and IRQ4 standard). Position 2, Com2-Asynchronous Communications Port 2 selected (2F8h and IRQ3).
J2	Diskette and Fixed Disk Drive Base-Address Select. This address selection option is available for special applications and under normal circumstances should not be changed. Position 1, Primary (Diskette1) Address Select (3F0h standard). Position 2, Secondary (Diskette2) Address Select (370h). "Diskette1 and Diskette2" are referencing the capabilities of using two addressable diskette controller boards, not diskette drives.
Note:	To change the setting, remove the shunt jumper room the socket, rotate it 180 degrees, and reinstall the jumper in the socket.

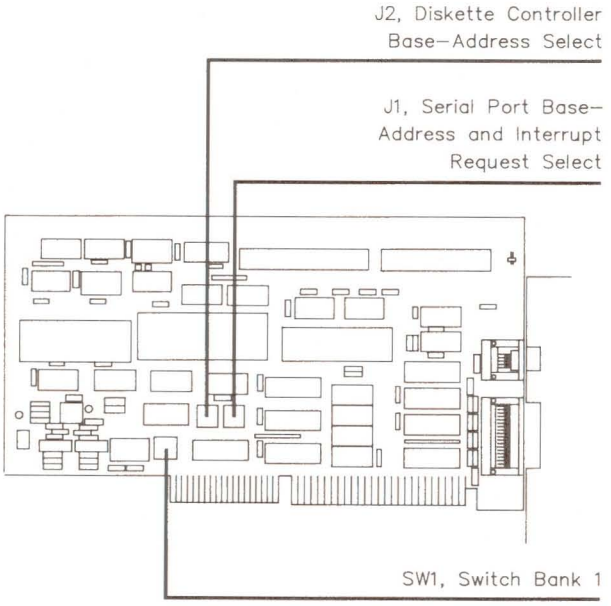


Figure 5-5. Multipurpose Fixed Disk Controller Board Jumper Locations

5.6 SWITCHES

The multipurpose fixed disk controller board and multipurpose controller board version 2 have four switches in one switch bank (SW1). These switches are described in Table 5-10.

Table 5-10. Multipurpose Fixed Disk Controller Board Switch Positions (SW1)

Number	Function
1	Fixed Disk Drive Enable. This switch allows the fixed disk drive port to be disabled. S1 = On, fixed disk drive port enabled (standard) S1 = Off, fixed disk drive port disabled.
2	Printer Enable. This switch allows the printer port to be disabled. This option prevents conflicts with I/O addresses 38Ch-38Fh when a multifunction board is installed that has a printer I/O port at these addresses. S2 = On, Parallel Printer Port enabled (standard) S2 = Off, Parallel Printer Port disabled.
3 (See Note)	Serial Port disable. Allows the serial port to be disabled. S3 = On, Serial Port Enabled (Standard) S3 = Off, Serial Port Disabled
4	Reserved Always Off.

Note: This function is available only on revision level G (or later) multipurpose fixed disk controller boards.

5.7 CONNECTORS

The connector descriptions for both the multipurpose controller board and multipurpose fixed disk controller boards are described in this section.

Table 5-11 lists the connectors and the number of table that contains the signal description for each connector. Tables 5-12 through 5-16 contain the signal descriptions for each controller board connector.

Figure 5-6 shows the multipurpose controller board connectors and jumpers. Figure 5-7 shows the multipurpose fixed disk controller board connectors and jumpers.

The multipurpose controller board signals used by diskette drives and fixed disk drive backup are listed in Table 5-17.

NOTE: Pin 34 of the 34-conductor control cable is implemented as the DISKETTE CHANGE- signal. Diskette drives that use this pin for DRIVE READY- do not work.

Table 5-11. Controller Connectors

Connector	Description	Location of Signal Description
J701	Asynchronous Communication Connector	Table 5-12
J502	Parallel Printer Connector	Table 5-13
J902	Fixed Disk Drive LED	Table 5-14
J901	Fixed Disk Drive Controller Host Adapter Connector	Table 5-15
J501	Diskette Drive Connector	Table 5-16

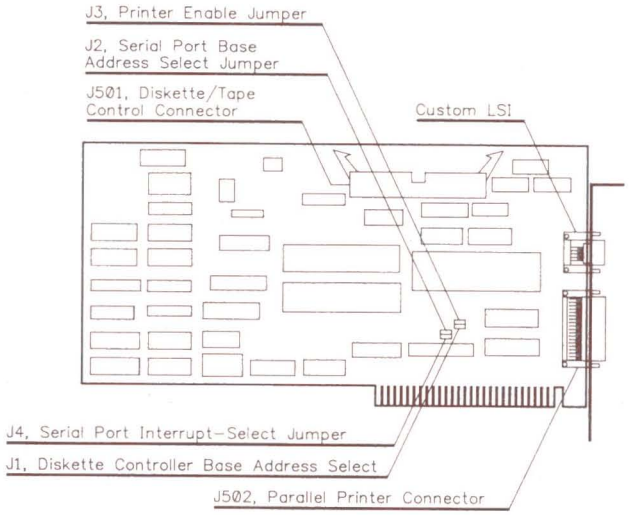


Figure 5-6. Multipurpose Controller Board Connector Locations

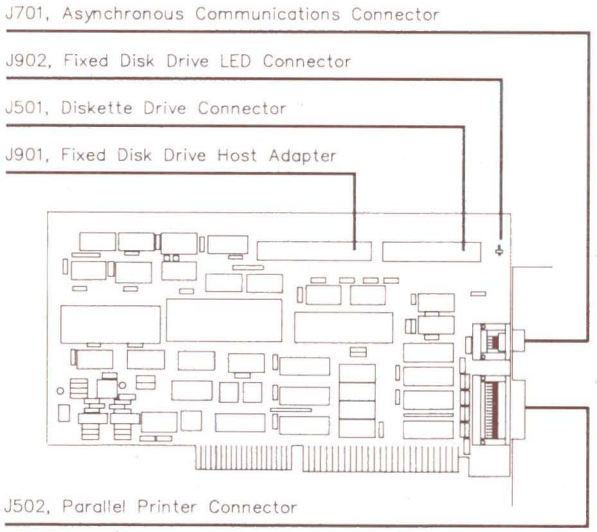


Figure 5-7. Multipurpose Fixed Disk Controller Board Connector Locations

Table 5-12. J701, 9-Pin Serial Connector Signals

Signal	Pin	I/O	Description
CARRIER DETECT (CD)	1	I	Modem signal indicating that a connection is established with another modem
CLEAR TO SEND SEND (CTS)	8	I	Modem signal indicating readiness to accept data
DATA SET READY (DSR)	6	I	Modem signal--it is online and can receive data
DATA TERMINAL READY (DTR)	4	O	Signal to a modem indicating that the computer is ready
RECEIVE DATA (RX)	2	I	Serial data receive line
REQUEST TO SEND (RTS)	7	O	Signal to a modem to request a transmission
RING INDICATOR (RI)	9	I	Modem signal indicating that it is receiving a ringing signal from the phone line
SIGNAL GROUND	5	- -	- -
TRANSMIT DATA (TX)	3	O	Serial data sent to modem

Note: All signal levels are RS-232-C compatible.

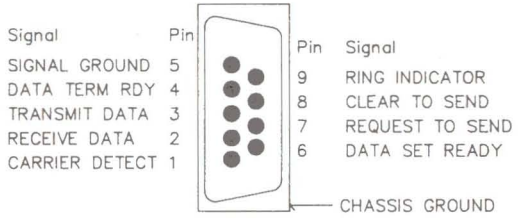


Figure 5-8. J701, 9-Pin Asynchronous Communications Connector

Table 5-13. J502, 25-Pin Parallel Printer Connector Signals

Signal	Pin	I/O	Description
ACKNOWLEDGE-	10	I	Data sent to printer has been received.
AUTO LINEFEED-	14	O	Instructs printer to automatically feed one line of paper after receiving a carriage return.
BUSY	11	I	Active-high signal indicating that the printer cannot receive data due to printing, offline, or error conditions.
DATA BIT 0	2	O	Signals transmit data to printer in 8-bit parallel format.
DATA BIT 1	3	O	
DATA BIT 2	4	O	
DATA BIT 3	5	O	
DATA BIT 4	6	O	
DATA BIT 5	7	O	
DATA BIT 6	8	O	
DATA BIT 7	9	O	
ERROR-	15	I	Indicates a printer error condition such as out-of-paper.
SIGNAL GROUND	18	-	Return conductors for all signals.
	19	-	
	20	-	
	21	-	
	22	-	
	23	-	
	24	-	
	25	-	

(Continued)

Table 5-15. (Continued)

Signal	Pin	I/O	Description
DD8 DD9 DD10 DD11 DD12 DD13 DD14 DD15	4 6 8 10 12 14 16 18	I/O I/O I/O I/O I/O I/O I/O I/O	Data bit 8-15. Most-significant eight bits for data and status communication between the controller and the host. DD15 is the most-significant bit of this byte.
DIOW-	23	O	I/O write. Active when the host writes a control byte or data word to the controller.
DIOR-	25	O	I/O read. Active when the host reads a status byte or data word from the controller.
I/O16CS-	32	I	Chip Select 16. Chip select used to signal the processor that the current I/O cycle is a 16-bit, single wait-state cycle.
IRQ14	31	I	Interrupt Request 14. Asserted by the controller to interrupt the processor upon completion of a fixed disk operation.
RST-	1	O	Reset. This signal resets the controller to the initial power-on condition.
SIGNAL GROUND	2,19, 22,24, 26,30,40	-	Return conductor.

Note: Pins 20, 21, 27, 29, and 34 are not connected.

Signal	Pin		Pin	Signal
RST–	1	■ ■	2	SIGNAL GROUND
DD7	3	■ ■	4	DD8
DD6	5	■ ■	6	DD9
DD5	7	■ ■	8	DD10
DD4	9	■ ■	10	DD11
DD3	11	■ ■	12	DD12
DD2	13	■ ■	14	DD13
DD1	15	■ ■	16	DD14
DD0	17	■ ■	18	DD15
SIGNAL GROUND	19	■ ■	20	KEY
RESERVED	21	■ ■	22	SIGNAL GROUND
DIOW–	23	■ ■	24	SIGNAL GROUND
DIOR–	25	■ ■	26	SIGNAL GROUND
RESERVED	27	■ ■	28	DALE
RESERVED	29	■ ■	30	SIGNAL GROUND
IRQ14	31	■ ■	32	IOCS16–
A1	33	■ ■	34	RESERVED
A0	35	■ ■	36	A2
CS1FX–	37	■ ■	38	CS3FX–
ACTIVE–	39	■ ■	40	SIGNAL GROUND

Figure 5-11. J901, Fixed Disk Drive Controller Host Adapter Connector

Table 5-16. J501, Diskette Drive Controller Signal Connector Descriptions

Signal	Pin	I/O	Description
LOW DENSITY-	2	O	Selects HIGH or LOW density for 1.2-MB diskette drives. Not used on 360-KB diskette drives.
DIRECTION-	18	O	Selects the direction to step the head when a step pulse is issued.
DISKETTE CHANGE-	34	I	Indicates that the drive door has been opened.
DRIVE 1 SELECT- DRIVE 2 SELECT- DRIVE 4(TAPE)SELECT-	14 12 6	O O O	Allows the selection of a drive so that it can respond to the interface signals.
INDEX-	8	I	(Diskette) Indicates to the drive controller that the media index opening is under the index sensor.
MOTOR1 ON-	10	O	Activates the drive motor.
MOTOR2 ON-	16	O	Activates the drive motor.
READ DATA-	30	I	This is the data-stream read from the drives and contains clock and data signals.
SIDE SELECT-	32	O	Selects Side 0 (Head 0) or Side 1 (Head 1).
STEP-	20	O	(Diskette) Tells the drive to step the heads one track.
TRACK 00-/BUSY-	26	I	(Diskette) Indicat- to the controller that the heads are at Track 0.
WRITE DATA-	22	O	This stream of data is written to the drive when WRITE GATE- signal is enabled.
WRITE GATE-	24	O	Enables the drive's write circuits so data from the WRITE DATA- signal is written.
WRITE PROTECT-	28	I	Indicates to the drive controller that the media is write protected.

Table 5-13. (Continued)

Signal	Pin	I/O	Description
INITIALIZE PRINTER-	16	O	Initializes the printer and clears the print buffer. This signal should remain active for at least 500 us.
PAPER END	12	I	Indicates that the printer is out of paper.
SELECT	13	I	Indicates that the printer is selected and online.
SELECT IN-	17	O	Selects the printer and enables it to accept data.
STROBE-	1	O	On high-to-low transition, causes data present on DATA BIT lines to be loaded into printer. STROBE- pulse width must be a minimum of 500 ns. Data must be setup a minimum of 500 ns before the high-to low transition and held a minimum of 500 ns after the low-to-high transition.

Note: All signals are TTL-level.

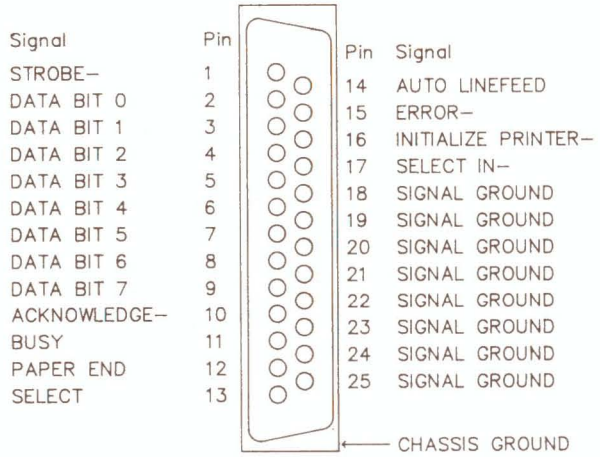


Figure 5-9. J502, 25-Pin Parallel Printer Connector

Table 5-14. J902, Fixed Disk Drive Controller LED Indicators

Signal	Pin	I/O	Description
LEDANODE	1		+5 VDC source for the fixed disk drive LED indicator.
- -	2		Reserved
ACTIVE-	3	O	Indicates that the fixed disk drive is being accessed. This line is used to drive an activity LED indicator that lights when the drive is activated.
- -	4		Reserved

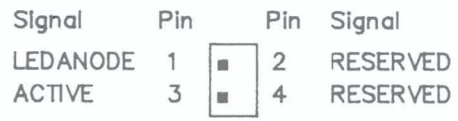


Figure 5-10. J902, Fixed Disk Drive Controller LED Indicators Connector

Table 5-15. J901, Fixed Disk Drive Controller Host Adapter Connector Signal Descriptions

Signal	Pin	I/O	Description
ACTIVE-	39	I	Active-low signal indicating that the fixed disk drive LED indicator is on and the fixed disk drive is being accessed.
CS1FX-	37	O	Chip Select 1Fx. Chip select decoded from the address bus and gated with AEN to select the controller registers at addresses 1F0h and 1F7h.
CS3FX-	38	O	Chip Select 3Fx. Chip select decoded from the address bus and gated with AEN to select the controller registers at addresses 3F6h through 3F7h.
DA0 DA1 DA2	35 33 36	O	Address A0-A2. Buffered address lines from the address bus to the fixed disk drive controller.
DALE	28	O	Address latch enable. Signals that address bus signals are stable and valid.
DD7 DD6 DD5 DD4 DD3 DD2 DD1 DD0	3 5 7 9 11 13 15 17	I/O I/O I/O I/O I/O I/O I/O I/O	Data bit 0-7. Least-significant eight bits of the 16-bit data bus for data and status communication between the controller and the host. D7 is the most-significant bit of this byte.

(Continued)

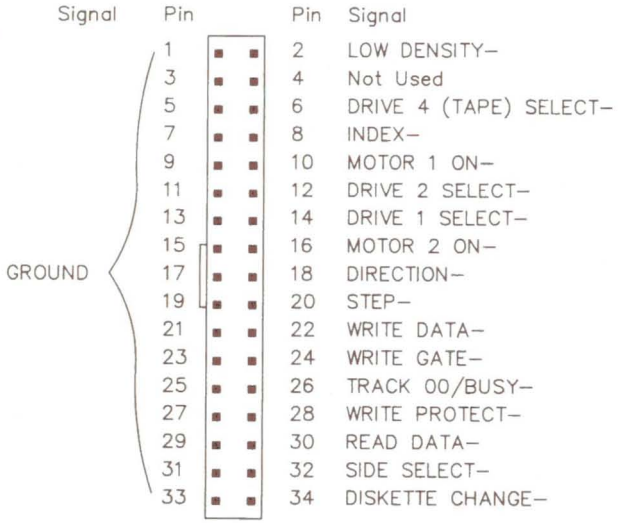


Figure 5-12. J501, Diskette Drive Controller Connector

Table 5-17. Multipurpose Fixed Disk Controller Signals Used by the Diskette Drives

Controller Pin	Function	Diskette Drive 1 Pin	Function (Note 1)	Diskette Drive 2 Pin	Function	Fixed Disk Drive Back-up Pin	Function
2	DENSITY-	2	DENSITY- (Note 2)	2	DENSITY-	2	DENSITY-
4	Not used	4	Not used	4	Not used	4	Not used
6	DRIVE 4 (TAPE) SELECT-	6	DRIVE 4 SELECT-	6	DRIVE 4 SELECT-	6	DRIVE 4 SELECT-
8	INDEX-	8	INDEX-	8	INDEX-	8	INDEX-
10	MOTOR 1 (A) ON-	10	MOTOR 2 ON-(Note 3)	10	MOTOR 1 ON-	10	MOTOR 2 ON-
12	DRIVE 2 (B) SELECT-	12	DRIVE 1 SELECT-(Note 3)	12	DRIVE 2 SELECT-	12	DRIVE 1 SELECT-
14	DRIVE 1 (A) SELECT-	14	DRIVE 2 SELECT-(Note 3)	14	DRIVE 1 SELECT-	14	DRIVE 2 SELECT-
16	MOTOR 2 (B) ON-	16	MOTOR 1 ON-(Note 3)	16	MOTOR 2 ON-	16	MOTOR 1 ON-
18	DIRECTION SELECT-	18	DIRECTION SELECT-	18	DIRECTION SELECT-	18	DIRECTION SELECT-
20	STEP-	20	STEP-	20	STEP-	20	STEP-
22	WRITE DATA-	22	WRITE DATA-	22	WRITE DATA-	22	WRITE DATA-
24	WRITE GATE-	24	WRITE GATE-	24	WRITE GATE-	24	WRITE GATE-
26	TRACK 00-/BUSY-	26	TRACK 00-/ BUSY-	26	TRACK 00-/ BUSY-	26	TRACK 00-/ BUSY-
28	WRITE PROTECT-	28	WRITE PROTECT-	28	WRITE PROTECT-	28	WRITE PROTECT-
30	READ DATA-	30	READ DATA-	30	READ DATA-	30	READ DATA-
32	SIDE SELECT-	32	SIDE SELECT-	32	SIDE SELECT-	32	SIDE SELECT-
34	DISKETTE CHANGE-	34	DISKETTE CHANGE-	34	DISKETTE CHANGE-	34	DISKETTE CHANGE-

Notes: 1. The order of the columns does not reflect the order of the connectors on the diskette disk drive cable.
2. Shaded areas denote functions unused on that drive.
3. The diskette drive cable interchanges pin 10 with pin 16 and pin 12 with pin 14 for Diskette Drive 1.

5.8 SCHEMATICS

The schematics for the multipurpose controller board are shown in Figures 5-13. Schematics for the multipurpose fixed disk controller board are shown in Figure 5-14. Compaq Computer Corporation does not guarantee the accuracy of the schematics. They are provided to aid in a general understanding of the operation of the controller.

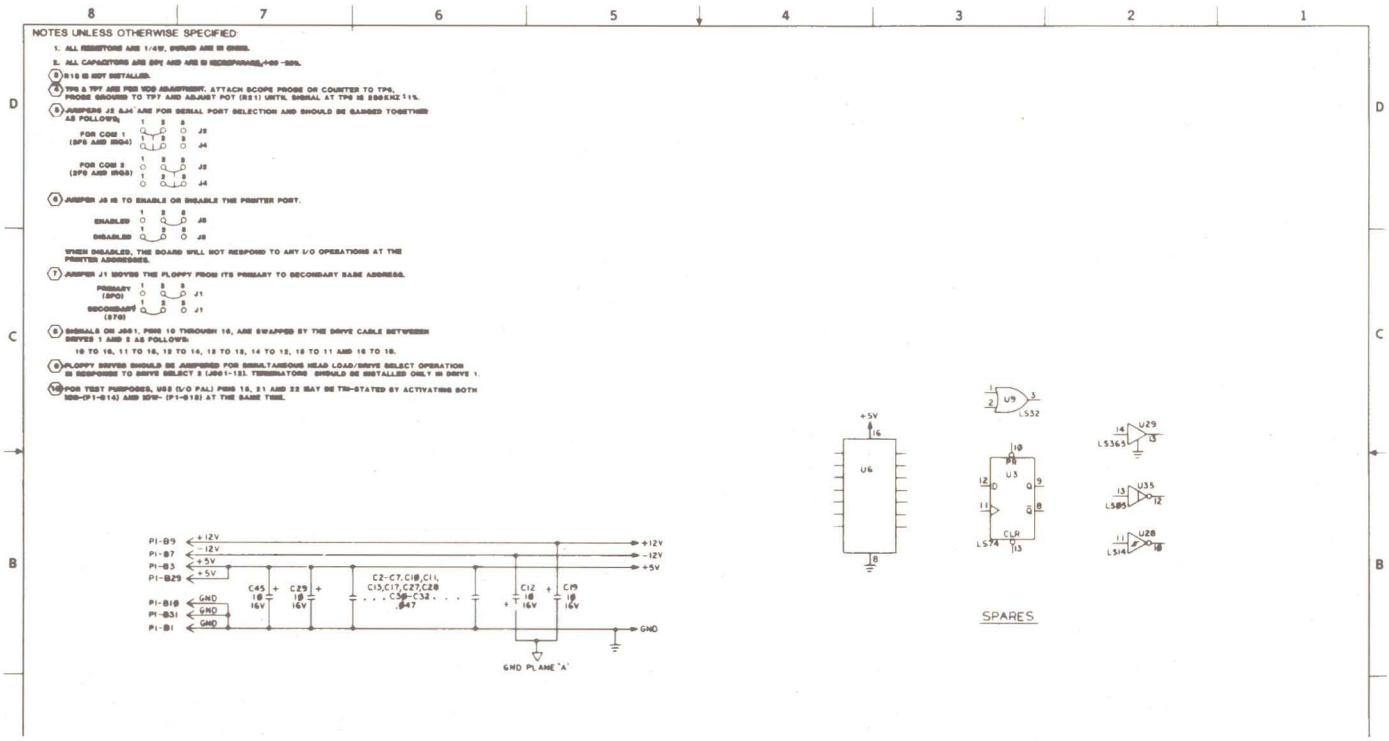


Figure 5-13. Multipurpose Controller Board Schematics (Page 1 of 4)

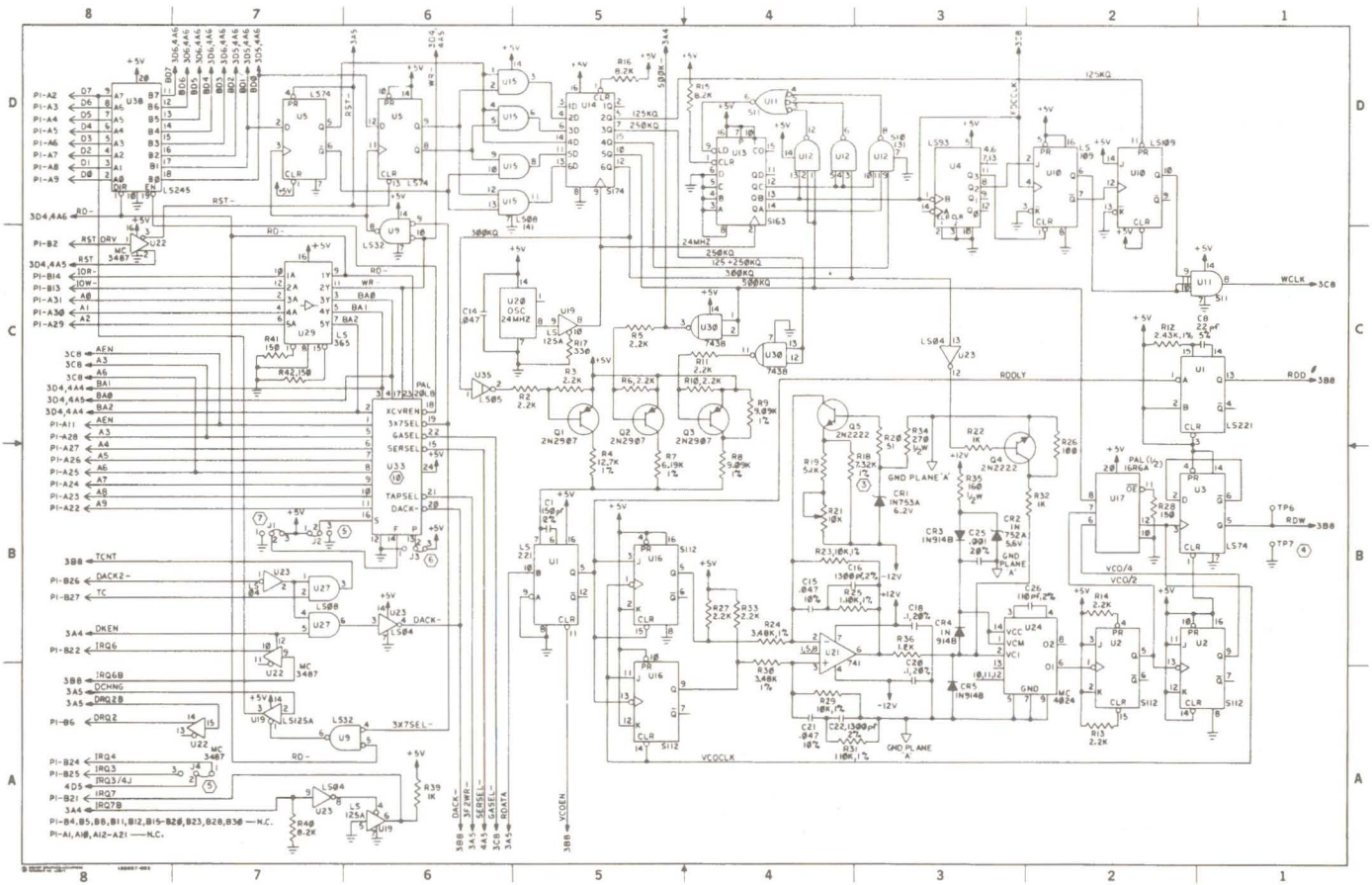


Figure 5-13. Multipurpose Controller Board Schematics (Page 2 of 4)

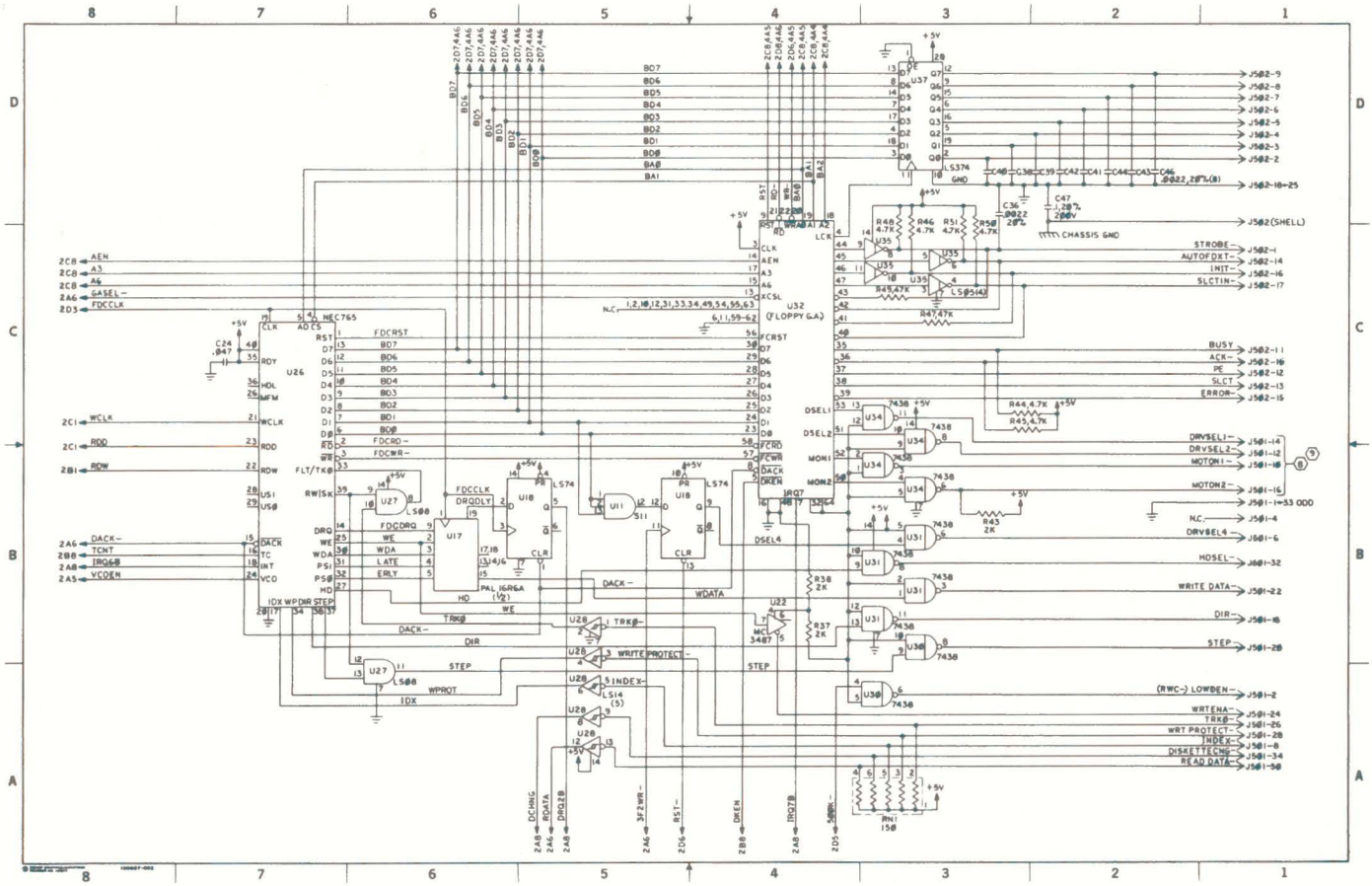


Figure 5-13. Multipurpose Controller Board Schematics (Page 3 of 4)

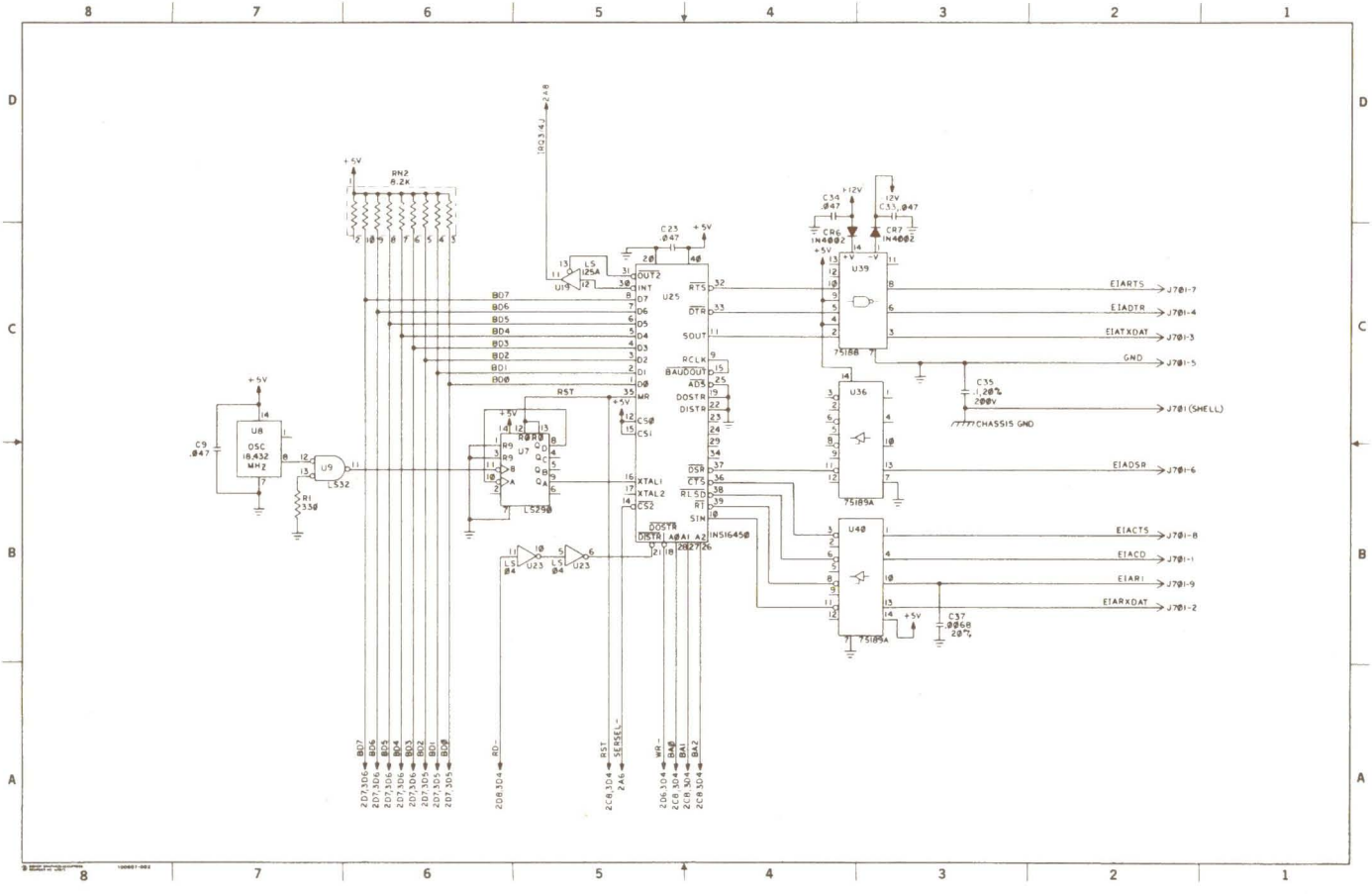


Figure 5-13. Multipurpose Controller Board Schematics (Page 4 of 4)

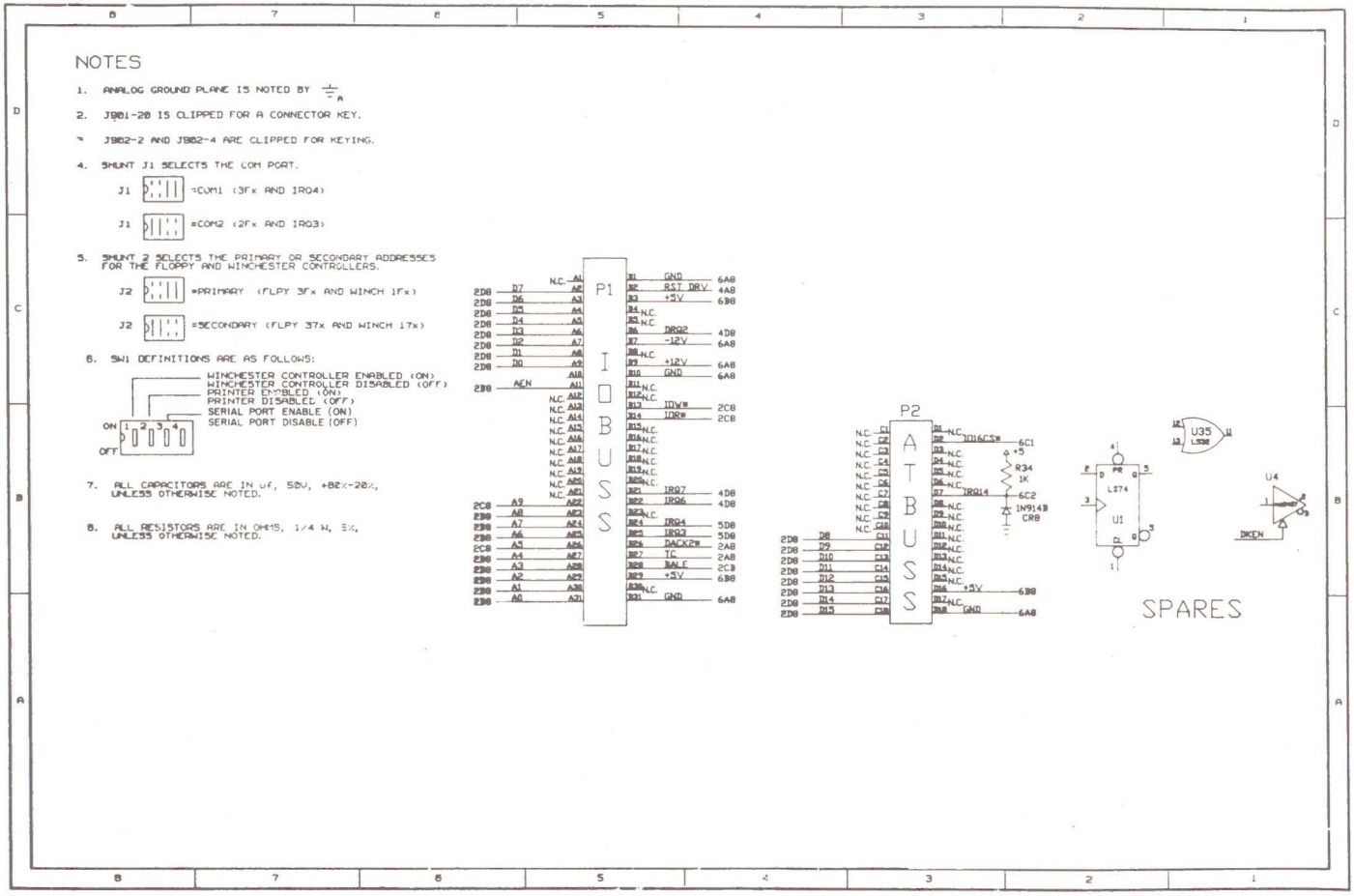


Figure 5-14. Multipurpose Fixed Disk Controller Board Schematics (Page 1 of 6)

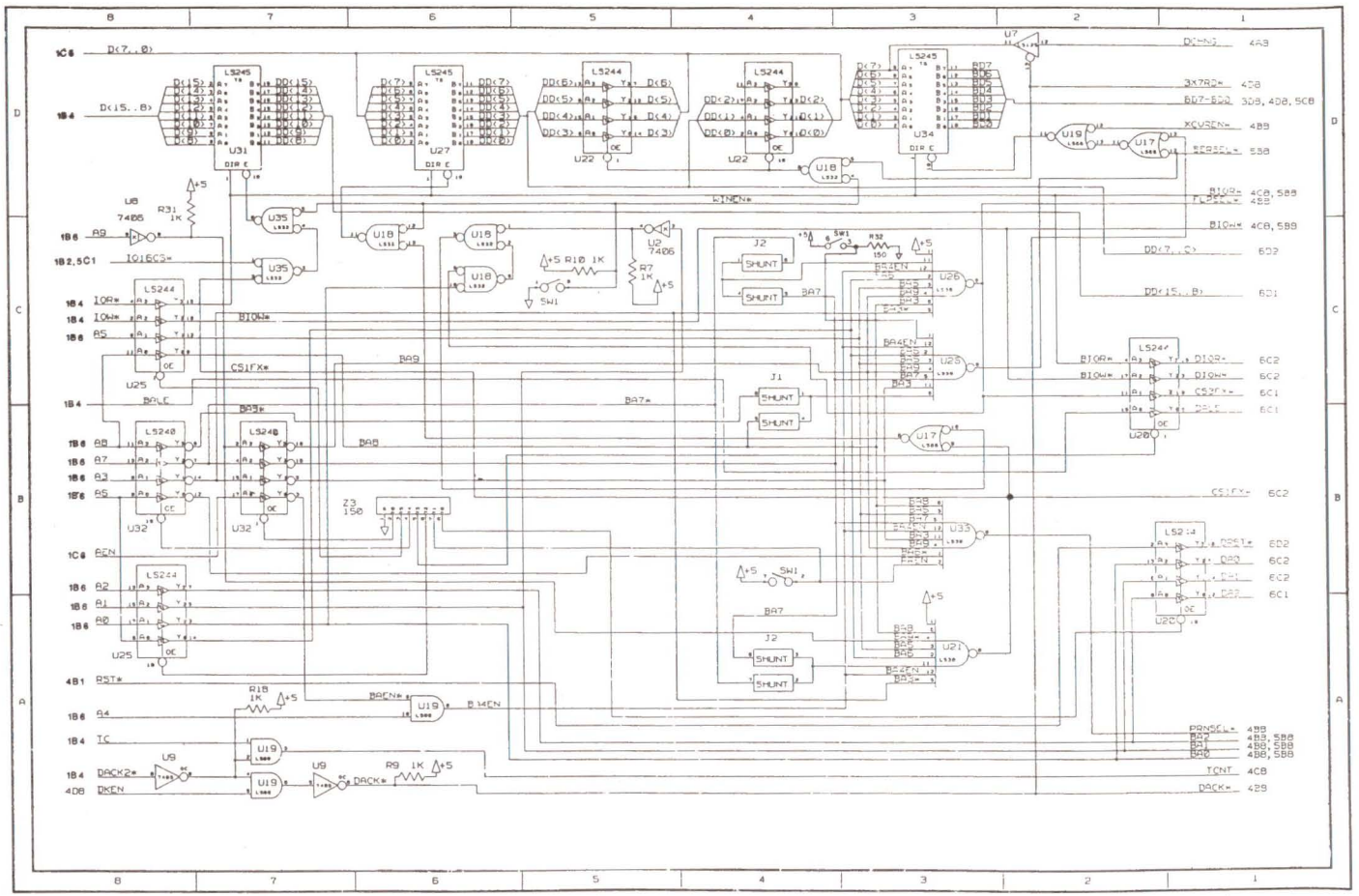


Figure 5-14. Multipurpose Fixed Disk Controller Board Schematics (Page 2 of 6)

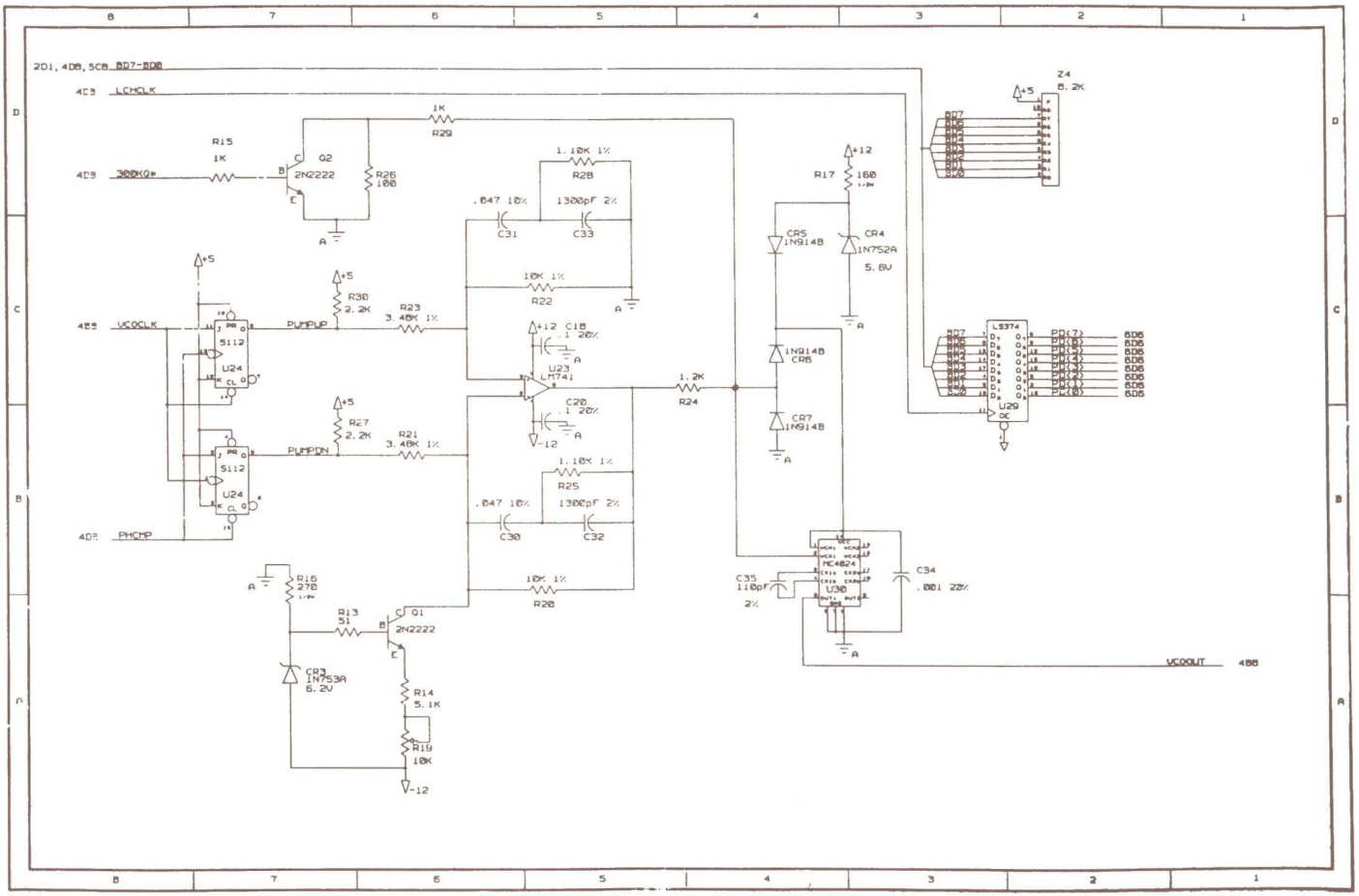


Figure 5-14. Multipurpose Fixed Disk Controller Board Schematics (Page 3 of 6)

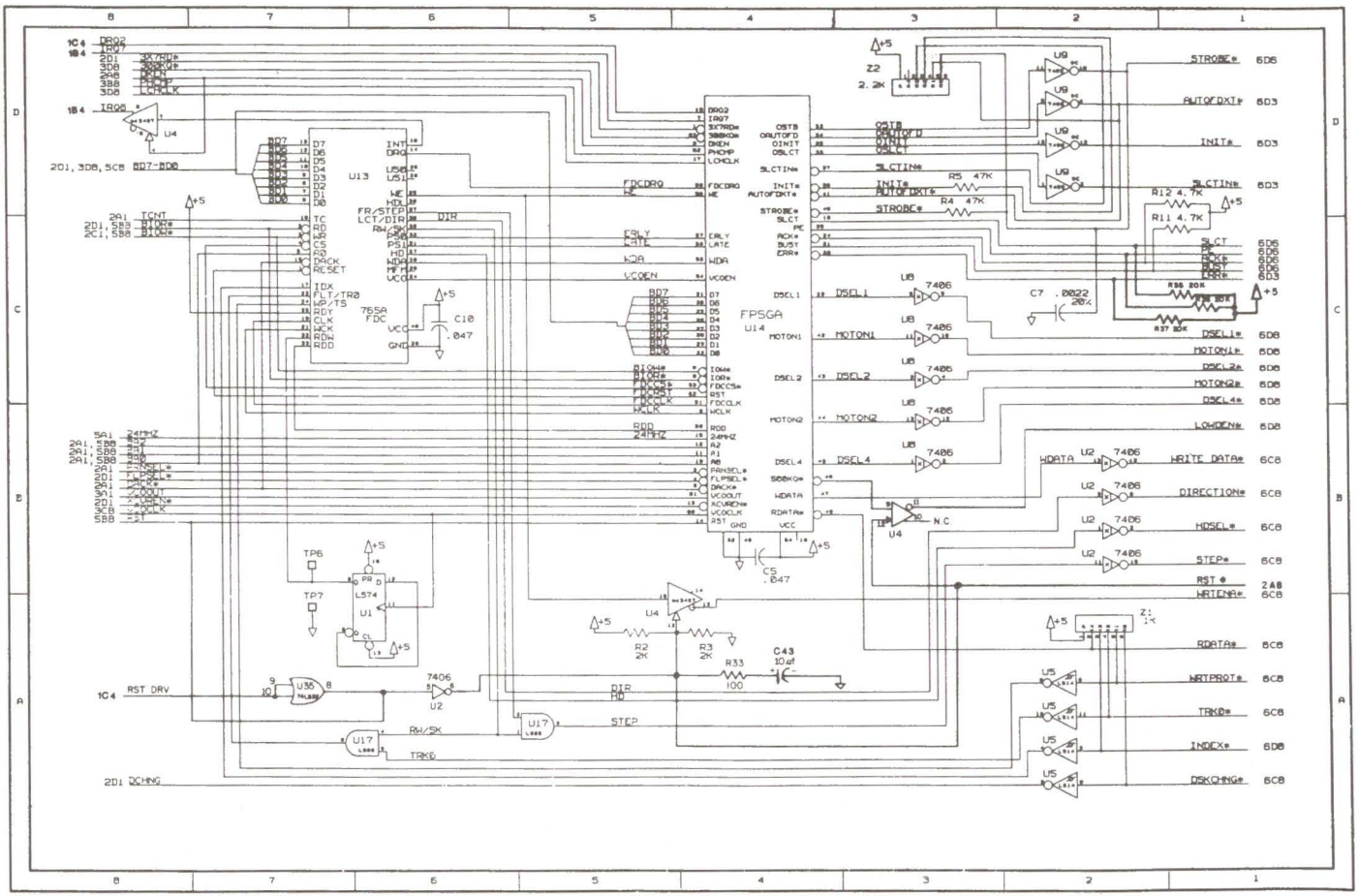


Figure 5-14. Multipurpose Fixed Disk Controller Board Schematics (Page 4 of 6)

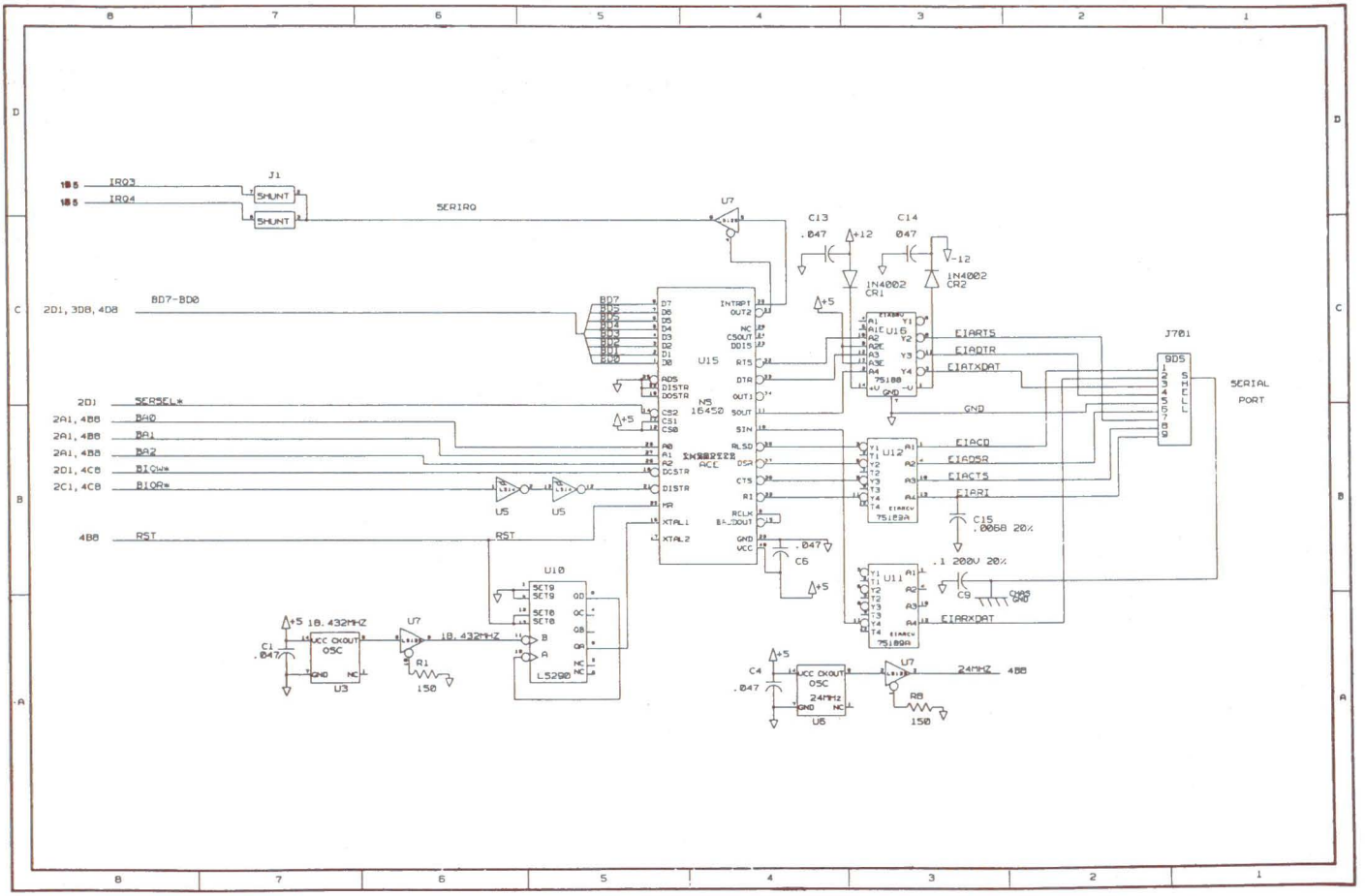


Figure 5-14. Multipurpose Fixed Disk Controller Board Schematics (Page 5 of 6)

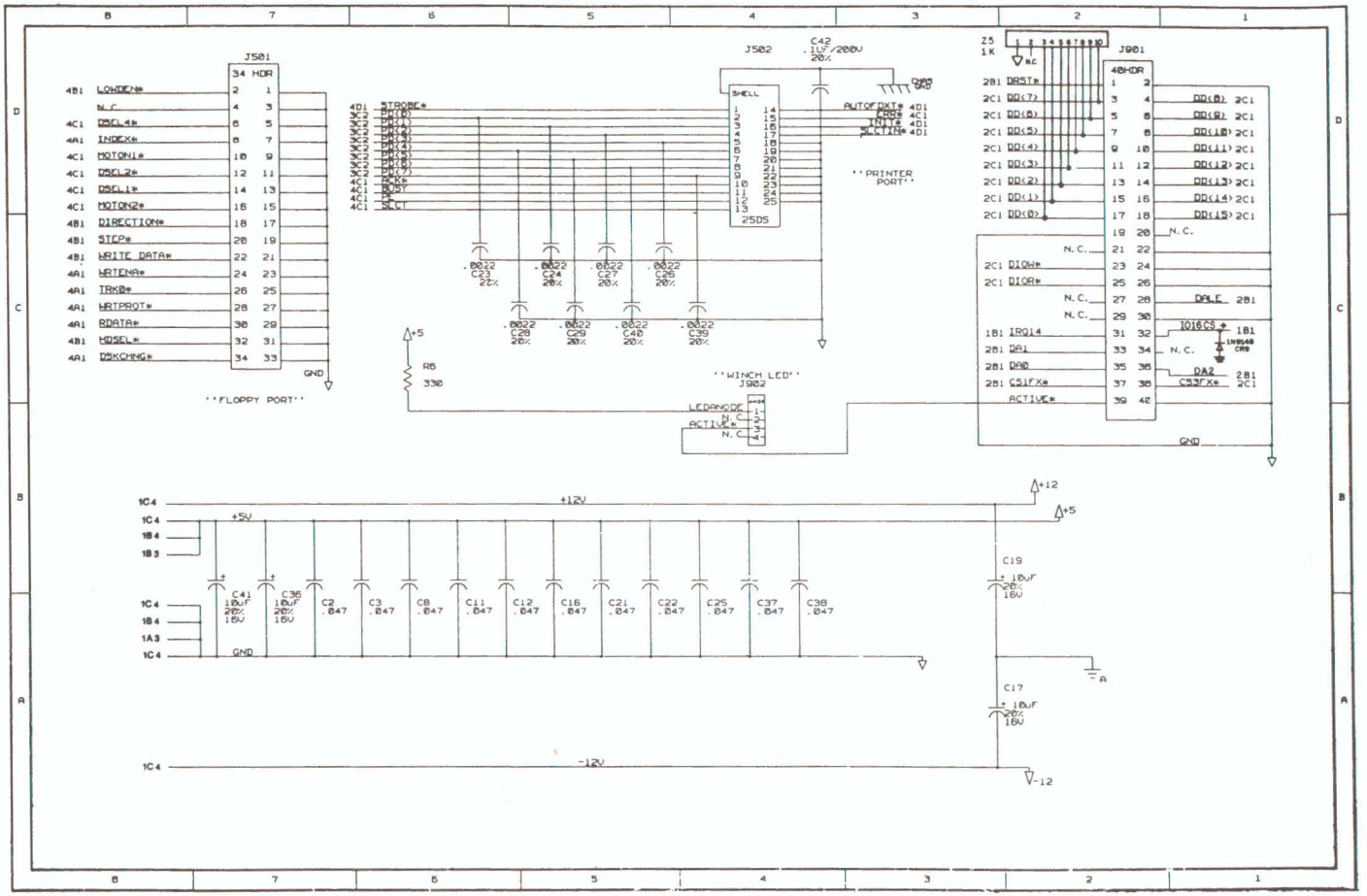


Figure 5-14. Multipurpose Fixed Disk Controller Board Schematics (Page 6 of 6)

Chapter 6

FIXED DISK DRIVE CONTROLLER BOARD

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CHAPTER 6
FIXED DISK DRIVE CONTROLLER BOARD

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FIXED DISK DRIVE CONTROLLER BOARD

6.1 INTRODUCTION

This chapter describes the fixed disk controller architecture and programming features for both the fixed disk drive controller board and the integrated fixed disk drives used in the COMPAQ DESKPRO 286.® Much of the information applies to both the integrated controller drives and the separate controller board. Information that applies only to intergrated drives is noted in the text.

The fixed disk drive controller board controls the functions of one or two fixed disk drives that use the ST506 interconnection standard. The fixed disk drive controller board has the following features:

- Plugs directly into an expansion slot in the COMPAQ DESKPRO 286® or COMPAQ PORTABLE 286® Personal Computer
- Transfers 16-bit data with high-speed programmed I/O instructions from the host
- Generates 17, 512-Kbyte sectors per track
- Incorporates 32-bit ECC polynomial for error detection and correction
- Generates overlapped seeks for buffered-step fixed disk drives
- Has on-board diagnostics

Figure 6-1 shows the functional block diagram.

The Fixed Disk Drive Controller Board is an I/O-mapped device. Table 6-1 shows the I/O addresses used to access the fixed disk drive controllers.

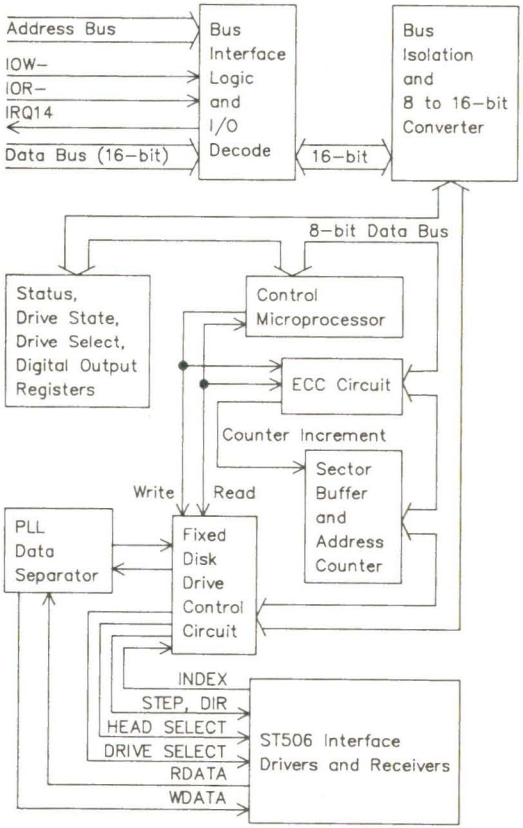


Figure 6-1. Fixed Disk Drive Controller Board Functional Block Diagram

6.2 FIXED DISK CONTROLLER PROGRAMMING

All fixed disk drive systems are fully compatible, which means that the I/O addresses, registers, and command structures are identical. The following paragraphs present the information that is common to all fixed disk drive systems.

Registers

Table 6-1 lists the standard and alternate I/O addresses for a fixed disk drive controller.

Table 6-1. Fixed Disk Drive Controller I/O Addresses

I/O Address 1	2	R/W	Register
1F0h	170h	R/W	DATA
1F1h	171h	R	ERROR
1F1h	171h	W	WRITE PRECOMPENSATION CYLINDER
1F2h	172h	R/W	SECTOR COUNT
1F3h	173h	R/W	SECTOR NUMBER
1F4h	174h	R/W	CYLINDER LOW
1F5h	175h	R/W	CYLINDER HIGH
1F6h	176h	R/W	SECTOR SIZE/DRIVE HEAD
1F7h	177h	R	STATUS
1F7h	177h	W	COMMAND
3F6h	376h	R	ALTERNATE STATUS
3F6h	376h	W	DRIVE CONTROL
3F7h	377h	R	DRIVE ADDRESS (See Note)
3F7h	377h	W	Not used for fixed disk

Note: Only bits D<6..0> are resident on the fixed disk drive controller. Bit <7> of this I/O address is resident on the diskette/tape controller.

DATA (1F0h)

All data to the fixed disk drive controller pass through the DATA register. The DATA register is also the port to which the sector table is transferred during format commands. All transfers are high-speed 16-bit I/O operations except for error correction code (ECC) bytes transferred during READ/WRITE LONG commands.

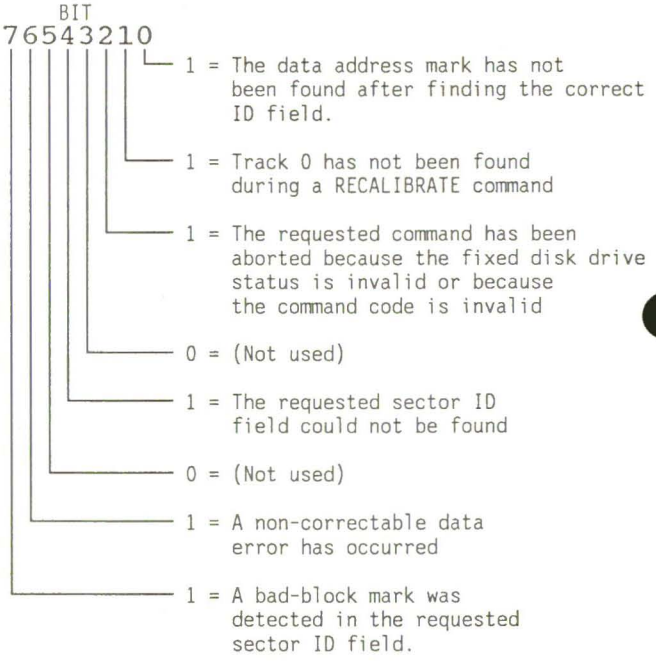
ERROR (1F1h, READ-ONLY)

The ERROR register contains error status from the last command executed by the fixed disk drive controller. The contents of this register are valid:

- When the error bit (ER) is set in the STATUS register
- When the fixed disk drive controller has completed execution of its internal diagnostics.

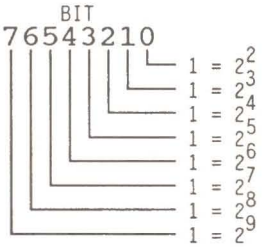
The contents of the ERROR register are interpreted as a diagnostic status byte after the execution of a diagnostic command or when the system is initialized.

The format of the Error register byte is shown below.



WRITE PRECOMPENSATION CYLINDER (1F1h, WRITE-ONLY)

The WRITE PRECOMPENSATION CYLINDER register defines the cylinder on which write precompensation begins. Precompensation time-shifts write data bits to help negate an opposite shift induced by the magnetic recording process. The controller multiplies the value in the register by 4, giving the bits of this register greater than usual value, or "weight" (see diagram).



The following tabulation gives some bit values and the resulting starting cylinders for write precompensation:

Bits	Starting Cylinder
00000001	4
00000010	8
00000100	16
00001000	32
00010000	64
00100000	128
01000000	256
10000000	512

SECTOR COUNT (1F2h)

The SECTOR COUNT register defines either the number of sectors of data to be read or written, or the number of sectors per track for format commands. If the value in this register is zero, a count of 256 sectors is specified. The sector count is decremented as each sector is read. The SECTOR COUNT register contains the number of sectors left to access when an error occurs in a multi-sector operation.

During the INITIALIZE DRIVE PARAMETERS command, the SECTOR COUNT register contains the number of sectors per track.

SECTOR NUMBER (1F3h)

The SECTOR NUMBER register contains the starting sector number for any fixed disk drive access.

At the completion of each sector and at the end of the command, this register is updated to reflect the last sector correctly read or the sector on which an error occurred.

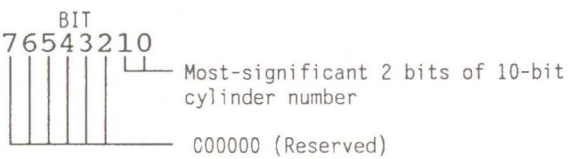
CYLINDER LOW (1F4h)
CYLINDER HIGH (1F5h)

The CYLINDER LOW and CYLINDER HIGH registers contain the starting cylinder number for any fixed disk drive access.

The CYLINDER LOW register is for the least-significant 8 bits of the 10-bit cylinder number. The 2 most-significant bits of the cylinder number, bits <0> and <1>, should be loaded into the CYLINDER HIGH register. Bit <1> of the CYLINDER HIGH register is the most-significant bit of the 10-bit cylinder address. At the completion of a command, these registers are updated to reflect the current cylinder number.

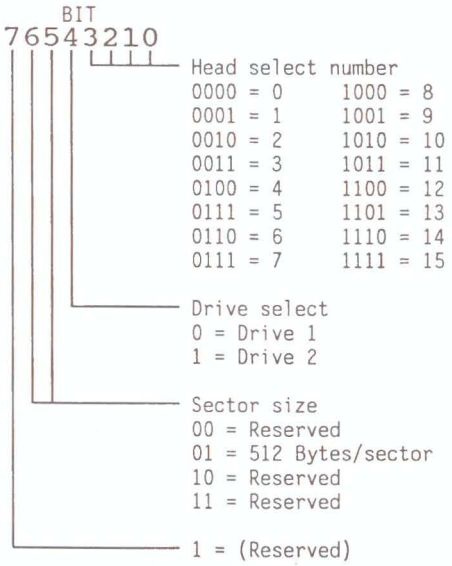
CYLINDER LOW Register:

CYLINDER HIGH Register:



SECTOR SIZE/DRIVE HEAD (1F6h)

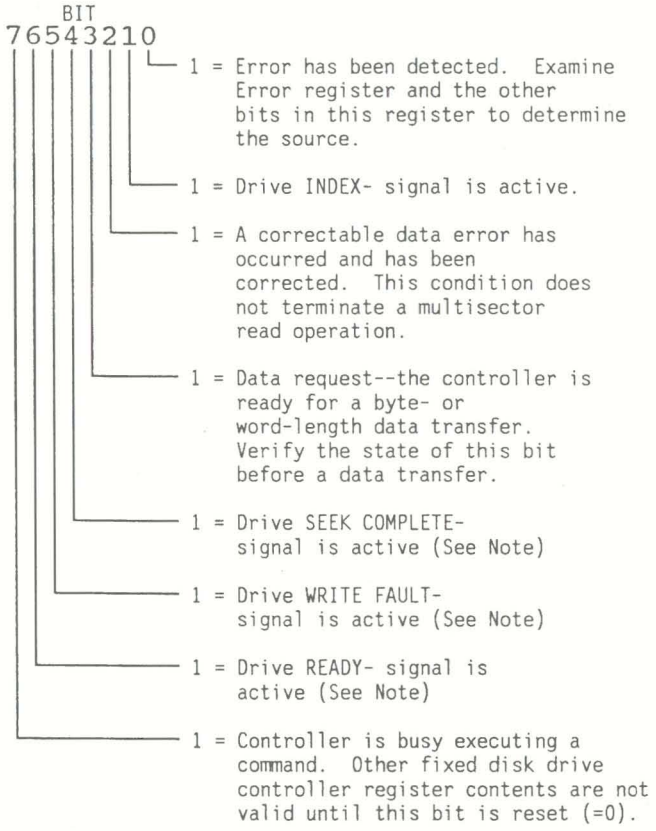
This register contains the parameters defined below:



NOTE: Setting bit <4> (Drive Select) to 1 when no drive is present may cause the remaining controller registers to fail to respond until Drive 1 is reselected.

STATUS (1F7h, READ-ONLY)

This register contains the fixed disk drive controller and fixed disk drive status. The contents of this register are updated at the completion of each command. If the Busy bit is set, no other bits are valid. Reading this register clears the hardware interrupt line, IRQ14.



NOTE: When an error exists, the state of the signals does not change until the error is read by the system.

COMMAND (1F7h, WRITE-ONLY)

Fixed disk drive controller commands are written to the COMMAND register. The following is a list of executable commands, command codes, and necessary command parameters.

Bit 7	6	5	4	3	2	1	0	Command Name
1	0	0	1	0	0	0	1	INITIALIZE DRIVE PARAMETERS
0	1	1	1	S	S	S	S	SEEK (Note 1)
0	0	0	1	S	S	S	S	RECALIBRATE (Note 1)
0	0	1	0	0	0	L	R	READ SECTORS (Notes 2 and 3)
0	0	1	1	0	0	L	R	WRITE SECTORS (Notes 2 and 3)
0	1	0	0	0	0	0	R	VERIFY SECTORS (Note 3)
0	1	0	1	0	0	0	0	FORMAT TRACK
1	0	0	1	0	0	0	0	EXECUTE CONTROLLER DIAGNOSTICS
1	1	1	0	1	1	0	0	IDENTIFY (Note 4)
1	1	1	0	0	1	0	0	READ SECTOR BUFFER (Note 4)
1	1	1	0	1	0	0	0	WRITE SECTOR BUFFER (Note 4)

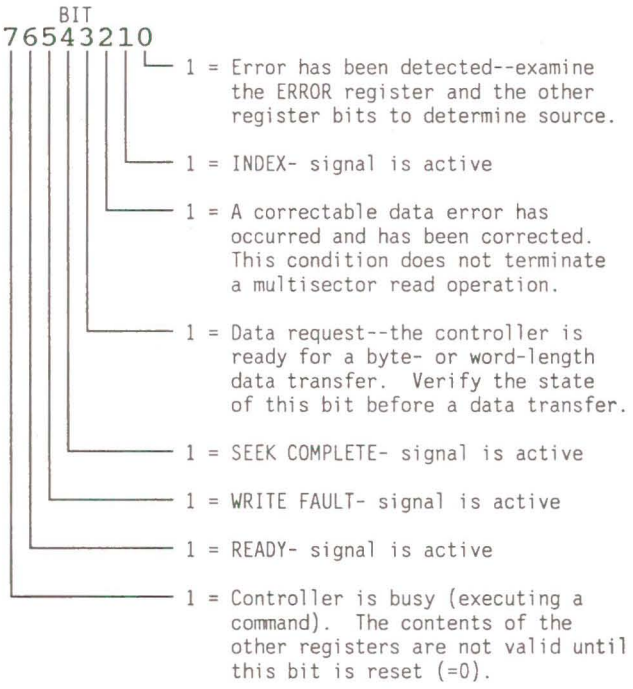
Notes: 1. S S S S = Step rate code (use following table):

0000	- 35.0 us	1000	- 4.0 ms
0001	- 0.5 ms	1001	- 4.5 ms
0010	- 1.0 ms	1010	- 5.0 ms
0011	- 1.5 ms	1011	- 5.5 ms
0100	- 2.0 ms	1100	- 6.0 ms
0101	- 2.5 ms	1101	- 6.5 ms
0110	- 3.0 ms	1110	- 3.2 us
0111	- 3.5 ms	1111	- 16.0 us

2. If L = 0, Read or Write is performed.
   If L = 1, Read Long or Write Long is performed.
3. If R = 0, Retries are enabled.
   If R = 1, Retries are disabled.
4. The 20-MB and 40-MB intergrated drives do not support the IDENTIFY, READ SECTOR BUFFER, or WRITE SECTOR BUFFER commands.

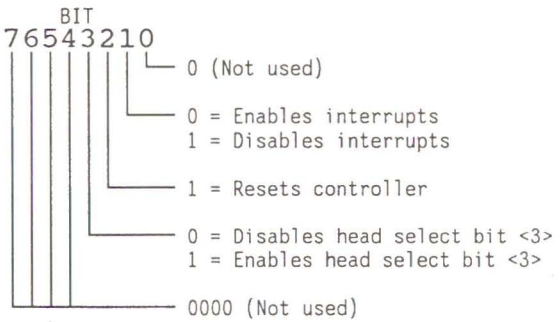
ALTERNATE STATUS (3F6h, Read Only)

The contents of this register are similar to those of the STATUS register, except in the timing and latch control of the specified signals. Reading this register does not clear any hardware conditions.



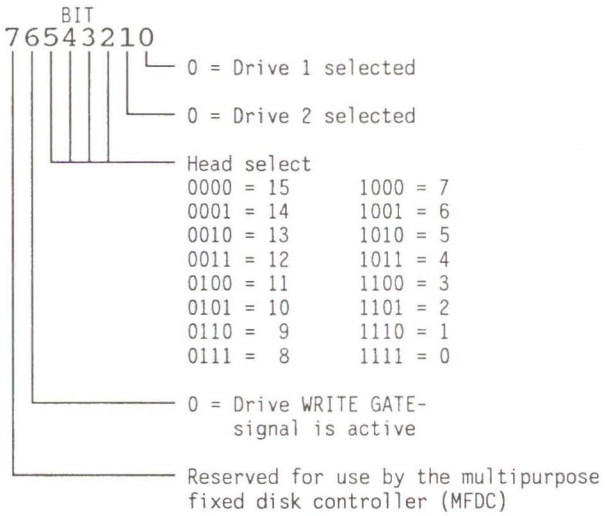
DRIVE CONTROL (3F6h, WRITE-ONLY)

The DRIVE CONTROL register defines several functions of the fixed disk drive controller.



DRIVE ADDRESS (3F7h, Read Only)

This register loops back the drive select and head select addresses of the most recently selected fixed disk drive. The bits in this port are as follows:



6.3 COMMAND INFORMATION

A command is issued to the controller by loading the pertinent registers with the needed parameters, enabling the fixed disk drive controller interrupt, and then writing the command code to a command register. Command execution begins when a command is written to a command register.

Table 6-2 lists the fixed disk drive controller commands.

Table 6-2. Fixed Disk Drive Controller Commands

Initialize Drive Parameters
SEEK
RECALIBRATE
READ SECTORS
READ LONG
WRITE SECTORS
WRITE LONG
VERIFY SECTORS
FORMAT TRACK
EXECUTE CONTROLLER DIAGNOSTIC
IDENTIFY
READ BUFFER
WRITE BUFFER

INITIALIZE DRIVE PARAMETERS

The INITIALIZE DRIVE PARAMETERS command enables the host to configure the controller to work with fixed disk drives that have different capacities and characteristics. Fixed disk drives 1 and 2 may be initialized for different drive parameters.

The SECTOR SIZE/DRIVE HEAD register must contain the maximum head number, and the SECTOR COUNT register must contain the number of sectors per track prior to executing this command.

The parameters loaded into the register prior to issuance of the command define the drive configuration for the specified fixed disk drive. If the INITIALIZE DRIVE PARAMETERS command is not issued, the fixed disk drive controller defaults to 17 sectors per track and 4 heads.

SEEK

The SEEK command initiates a SEEK to the track and selects the head specified. The fixed disk drive need not be formatted for a seek to execute properly. The controller supports buffered step seeks, allowing overlapped seeks on the drives.

After initiating a SEEK on one fixed disk drive, another command can be issued to the other drive. If a new command is received for a fixed disk drive with an outstanding SEEK, then the controller waits, with BUSY active, for the SEEK to complete before executing the new command. There is no time-out condition in the controller while waiting for buffered-step seeks to complete.

RECALIBRATE

The RECALIBRATE command moves the read/write heads to cylinder 0. If the fixed disk drive is unable to reach cylinder 0, the command is aborted with the error bit set in the STATUS register and the Track 0 bit set in the ERROR register.

The stepping-rate code included with this command does not have any effect on the recalibrate stepping, but is used as the stepping rate for any subsequent implied seeks executed by the controller.

READ SECTORS

The READ SECTORS command reads from 1 to 256 sectors as specified in the SECTOR COUNT register, beginning at the specified sector. If the fixed disk drive is not already on the requested track, an implied seek is performed at the stepping rate defined in the last Recalibrate command.

After reaching the specified track, the controller begins searching for the appropriate ID field. If retries are disabled, a maximum of 2 revolutions are taken and, if retries are enabled, 16 revolutions are taken before reporting an ID Not Found error. If the ID is read correctly, the data address mark must be recognized within a fixed number of bytes, or the Data Address Mark Not Found error will be reported.

After the data address mark is found, the data field is read, and the sector read is finished with either no error, a correctable data error, or a non-correctable data error, depending on whether or not the ECC bytes are correct for the preceding data field.

If an error occurs during a multiple-sector read, the read terminates at the sector where the error occurs. The system may then read the registers, determine what error has occurred, and on which sector. If the error was a non-correctable data error, the flawed data are still returned to the system.

READ LONG

A READ LONG command returns the data field and the ECC bytes contained in the data field of the desired sector.

During a READ LONG operation, the controller does not check the ECC bytes to determine if there has been any type of data error. The data bytes are read out of the sector buffer at the completion of the command, which is signaled by an interrupt. All data transfers are high-speed 16-bit operations and all ECC byte transfers on READ LONG commands are slower 8-bit operations. All the drive/controllers have 4 ECC bytes.

WRITE SECTORS

The WRITE SECTORS command writes from 1 to 256 sectors of data, as specified in the SECTOR COUNT register, beginning at the specified sector. If the fixed disk drive is not already on the requested track, an implied seek is performed at the stepping rate defined in the last RECALIBRATE command.

Once at the desired track, the controller begins searching for the appropriate ID field. If retries are disabled, a maximum of 2 revolutions are taken and, if retries are enabled, 16 revolutions are taken before reporting an ID Not Found error. If the ID is read correctly, the data loaded in the sector buffer are written to the data field of the sector, along with the approximate number of ECC bytes. If an error occurs during a multiple-sector write, the write terminates at the sector where the error occurs. The system may then read the registers, determine what error has occurred, and on which sector.

WRITE LONG

A WRITE LONG operation may be executed by setting the long bit in the command code. The WRITE LONG command writes the data field and the ECC bytes directly from the sector buffer; the controller does not generate the ECC bytes. All data transfers are high-speed 16-bit operations and all ECC byte transfers on Write Long commands are slower 8-bit operations. The 40-MB and 70-MB drive/controllers have 4 ECC bytes, and the 130-MB drive/controller has 7 ECC bytes.

VERIFY SECTORS

This command is identical to the READ SECTORS command, except that no data are transferred back to the system and no READ LONG operations are permitted. The read procedure described in the READ command is followed and any errors encountered are reported to the system.

FORMAT TRACK

The FORMAT TRACK command formats the track specified by the head and cylinder parameters in the registers. If the fixed disk drive is not already on the specified track, an implied SEEK is performed at the stepping rate defined in the last RECALIBRATE command. After reaching the specified track, the ID and data fields are written using the sector table in the sector buffer.

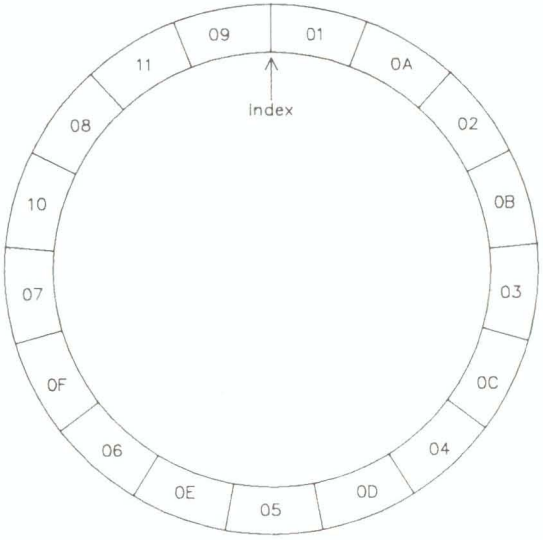
The sector table contains 2 bytes per sector on the track. The first byte is 00h if the sector is to be formatted normally, or 80h if the sector is to be formatted bad. The second byte is the logical sector number of the sector.

As soon as the fixed disk drive controller senses the index pulse from the fixed disk drive, formatting begins by writing the first physical sector with the logical sector number in the first entry of the sector table.

Subsequent physical sectors are formatted in turn from the sector table. The order of the sector table entries will correspond to the interleave factor of the track. Media defects may be marked bad on a sector level, allowing the remainder of the track to be used.

Once the command is issued, the sector table is output to the Data register, and additional bytes should be loaded into the buffer until it is full (512 bytes). Figure 6-2 shows the contents of a typical sector table for a 17-sector track with an interleave factor of 2 and sector 3 marked bad.

To format a fixed disk drive with more than 8 heads, recalibrate (INT 13h, AH = 11h) head 0, then format heads 0 through 7. Next, recalibrate head 8 and format heads 8 through 15.



Sector																			
00	01	00	0A	00	02	00	0B	80	03	00	0C	00	04	00	0D
00	05	00	0E	00	06	00	0F	00	07	00	10	00	08	00	11
00	09	dd	dd	dd	dd	dd	dd	dd	dd	dd	dd	dd	dd	dd	dd
dd	dd	dd	dd	dd	dd	dd	dd	dd	dd	dd	dd	dd	dd	dd	dd
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
dd	dd	dd	dd	dd	dd	dd	dd	dd	dd	dd	dd	dd	dd	dd	dd

Note: "dd" is a "don't care" byte used to make up a total of 512 bytes.

Figure 6-2. Typical Sector Table

EXECUTE CONTROLLER DIAGNOSTIC

This command performs the internal diagnostic tests implemented by the controller. The results of the test are reported to the ERROR register immediately after execution of the command. The value in the ERROR register should be viewed as an unique 8-bit code and not as the single-bit flags previously defined.

Table 6-3 lists the error codes and the corresponding explanation.

Table 6-3. Fixed Disk Drive Controller Error Codes

Error Code	Description
01h	No error detected
02h	Formatter device error
03h	Sector buffer error
04h	ECC circuitry error
05h	Controller microprocessor error

IDENTIFY

The IDENTIFY command allows the host to receive parameter information from the drive. When the command is issued, the controller gets the parameters from the drive, stores them in the sector buffer, sets the DRQ bit in the STATUS register, and allows the host to read the information out of the sector buffer. The parameter words in the buffer are described in Table 6-4.

Table 6-4. IDENTIFY Command Parameter Words

Word	Contents
0	General configuration
1	Number of fixed cylinders
2	Reserved
3	Number of heads
4	Number of unformatted bytes per physical track
5	Number of unformatted bytes per sector
6	Number of physical sectors per track
7	Reserved
.	
.	
.	
255	Reserved

Table 6-5 gives bit definitions of the general configuration word.

Table 6-5. Configuration Word Bits

Bit	Definition
<0>	Reserved
<1>	1=Hard sectored
<2>	1=Soft sectored
<3>	1=Not MFM encoded
<4>	1=Head switch time greater than 15 microseconds (us)
<5>	1=Spindle motor control option implemented
<6>	1=Fixed drive
<7>	1=Removable cartridge drive
<8>	1=Transfer rate less than or equal to 5 Mb/s
<9>	1=Transfer rate greater than 5 Mb/s, but less than or equal to 10 Mb/s
<10>	1=Transfer rate greater than 10 Mb/s
<11>	1=Rotational speed tolerance is greater than 0.5 percent
<12>	1=Data strobe offset option implemented
<13>	1=Track offset option implemented
<14>	1=Format speed tolerance gap required
<15>	0=Magnetic disk drive 1=Nonmagnetic disk drive

READ BUFFER

The READ BUFFER command allows the host to read the current contents of the controller's sector buffer. When this command is issued, the controller goes busy, sets up the sector buffer for a read operation, sets the data request bit (DRQ), and goes not busy. The host can then read as many as 512 bytes of data.

WRITE BUFFER

The WRITE BUFFER command allows the host to overwrite the contents of the controller's sector buffer with any data pattern desired. When this command is issued, the controller goes busy, sets up the sector buffer for a write operation, sets the data request bit (DRQ), and goes busy. The host can then write as many as 512 bytes of data.

Fixed Disk Drive Controller Error Reporting

The errors that are valid for each command are defined in the matrix below:

Command	BB	UD	ID	AC	TZ	AM	NR	WF	SC	CD	ER
Initialize Drive Parameters	–	–	–	–	–	–	V	V	V	–	–
Seek	–	–	V	V	–	–	V	V	V	–	V
Recalibrate	–	–	–	V	V	–	V	V	V	–	V
Read Sectors	V	V	V	V	–	V	V	V	V	V	V
Read Long	V	–	V	V	–	V	V	V	V	–	V
Write Sectors	V	–	V	V	–	–	V	V	V	–	V
Write Long	V	–	V	V	–	–	V	V	V	–	V
Verify Sectors	V	V	V	V	–	V	V	V	V	V	V
Format Track	–	–	V	V	–	–	V	V	V	–	V
Execute Controller Diagnostic	–	–	–	–	–	–	–	–	–	–	V
Identify	–	–	–	V	–	–	V	V	V	–	V
Read Buffer	–	–	–	–	–	–	–	–	–	–	–
Write Buffer	–	–	–	–	–	–	–	–	–	–	–
Invalid Command Code	–	–	–	V	–	–	–	–	–	–	V

Legend:

BB = Bad block detected
UD = An uncorrectable data error
ID = Requested ID not found
AC = An aborted command error
TZ = Track 0 not found error
AM = Data Address Mark not found
NR = Disk drive not ready detected
WF = Disk drive write fault detected
SC = Disk drive seek complete not detected
CD = A corrected data error
ER = The error bit in the Status register
V = Indicates that this error type is valid for this command

6.4 CONNECTORS

Tables 6-6 and 6-7 list the fixed disk drive connector pinouts and signal descriptions.

Figure 6-3 shows the J1, Fixed Disk Drive Control Connector.

Table 6-6. J1, Fixed Disk Drive Control Connector Signal Description

Signal	Pin	I/O	Description
DIRECTION IN-	34	O	Signal that defines the direction of motion of the heads when the fixed disk drive is executing a seek.
DRIVE SELECT 1-	26	O	Signal indicating that Fixed Disk Drive 1 is to respond to the control signals on the fixed disk drive control bus.
DRIVE SELECT 2-	28	O	Signal indicating that Fixed Disk Drive 2 is to respond to the control signals on the fixed disk drive control bus.
HEAD SELECT 2^0-	14	O	First and least-significant bit of the binary-coded head-select address.
HEAD SELECT 2^1-	18	O	Second bit of the binary-coded head-select address.
HEAD SELECT 2^2-	4	O	Third bit of the binary-coded head-select address.

(Continued)

Table 6-6. (Continued)

Signal	Pin	I/O	Description
INDEX-	20	I	Indicates the beginning of a track.
REDUCED WRITE CURRENT-/ HEAD SELECT 2^3-	2	O	This signal functions as the reduced write current signal or a head-select 2^3 bit. The control bit for this selection is in the fixed disk drive control register. In the reduced write current mode, this line, in conjunction with the WRITE GATE- signal, reduces the magnitude of the write current for writing on inner disk cylinders. In the head-select mode, this pin is the fourth and most significant bit of the head-select binary code.
READY-	22	I	When active together with SEEK COMPLETE-, this signal indicates that the fixed disk drive is ready to perform a read, write, or seek command.

(Continued)

TABLE 6-6. (Continued)

Signal Name	Pin	I/O	Description
Reserved	16	--	
Reserved	30	--	
Reserved	32	--	
SEEK COMPLETE-	8	I	Signals that the heads have settled on the specified track at the end of a track seek operation.
STEP-	24	O	Signal which causes the heads to move one track in the direction defined by the DIRECTION IN- signal.
TRACK 000-	10	I	Indicates that the heads are on track zero (000).
WRITE FAULT-	12	I	Indicates that a condition exists that may cause improper writing on the fixed disk and that writing is, therefore, inhibited.
WRITE GATE-	6	O	When active, allows data on the MFM WRITE DATA signal to be written on the fixed disk.

Note: All odd-numbered pins are Signal Ground.

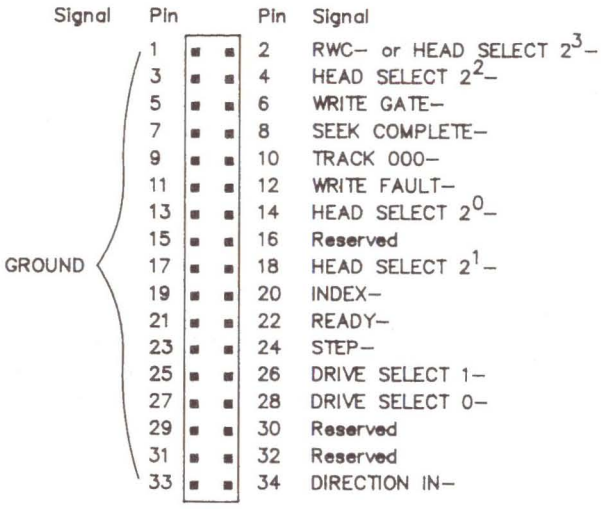


Figure 6-3. J1, Fixed Disk Drive Control Connector

Figure 6-4 shows the J2 and J3 fixed disk drive data connector.

Table 6-7. J2 and J3, Fixed Disk Drive Data Connector Signals

Signal Name	Pin	I/O	Signal Description
DRIVE SELECTED-	1	I	When active, indicates that the fixed disk drive has acknowledged being selected.
GROUND	2,4,6, 11,12, 15,16, 19,20,	--	Signal Ground
+MFM WRITE DATA	13	O	MFM encoded write data to be written to the fixed disk drive.
-MFM WRITE DATA	14	O	MFM encoded write data to be written to the fixed disk drive.
+MFM READ DATA	17	I	MFM encoded read data from the fixed disk drive.
-MFM READ DATA	18	I	MFM encoded read data from the fixed disk drive.
Reserved	3,5,7	--	
Spare	9,10	--	

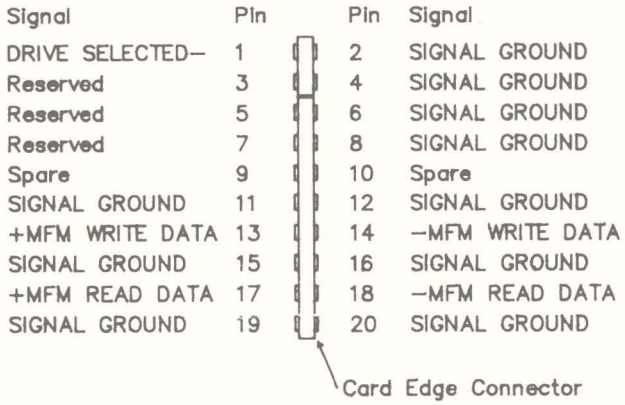


Figure 6-4. J2 and J3, Fixed Disk Drive Data Connector

6.5 SCHEMATICS

Figure 6-5 show the schematics for the fixed disk drive controller board. Compaq Computer Corporation does not guarantee the accuracy of the schematics. They are provided to aid in a general understanding of the system operation.

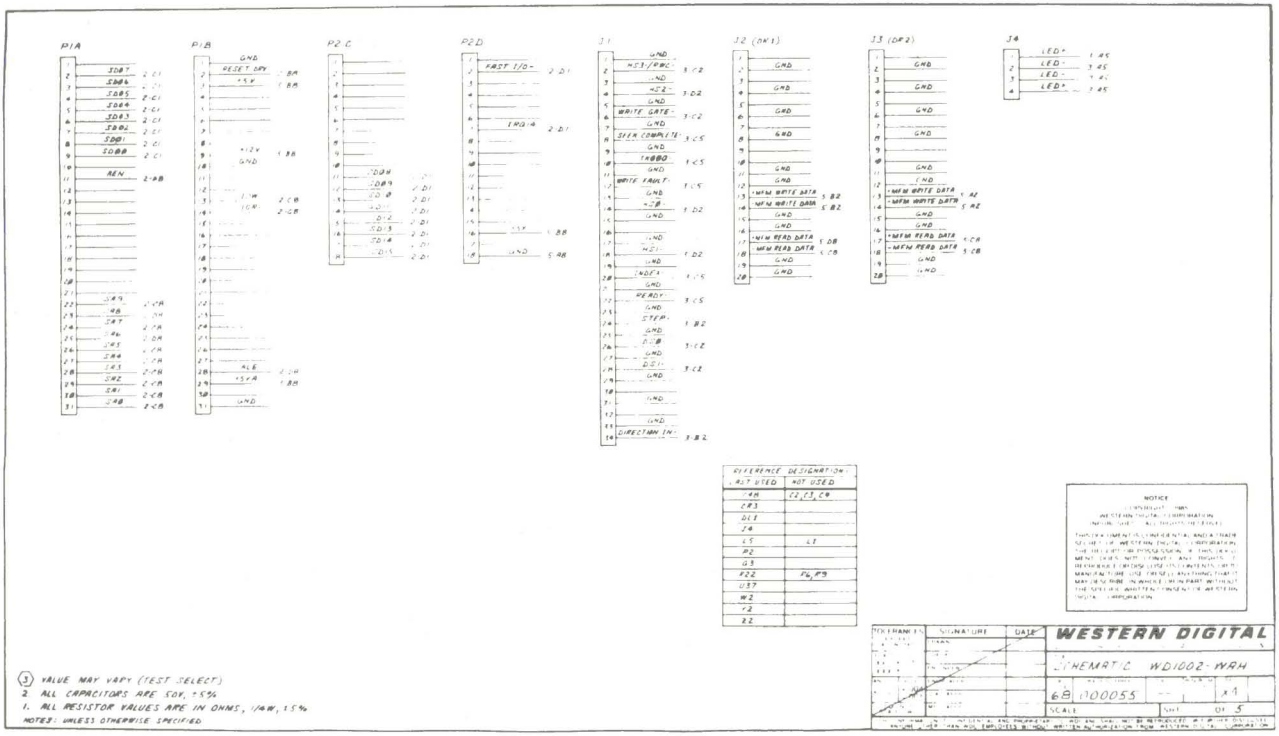


Figure 6-5. Fixed Disk Drive Controller Board Schematics (Page 1 of 5)

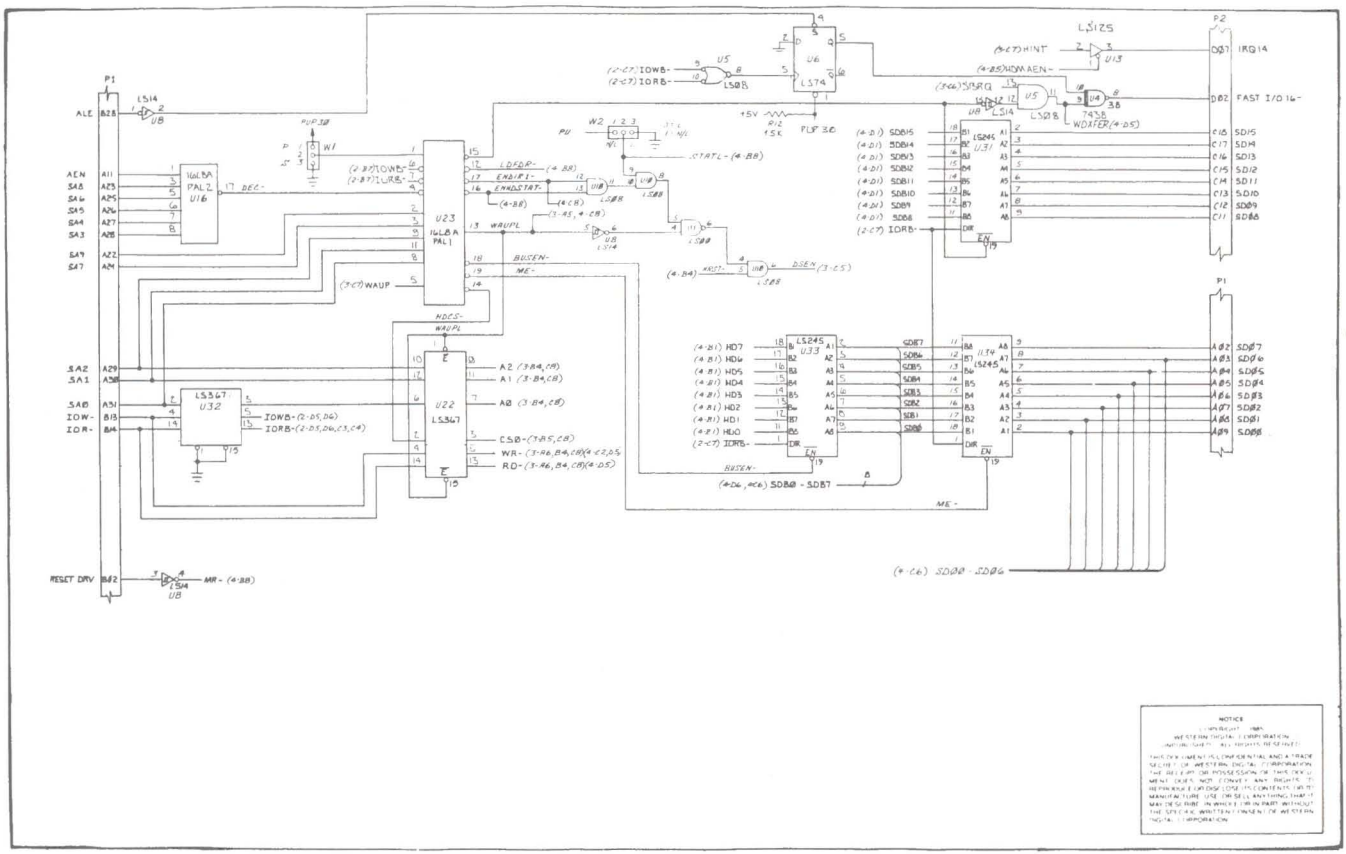


Figure 6-5. Fixed Disk Drive Controller Board Schematics (Page 2 of 5)

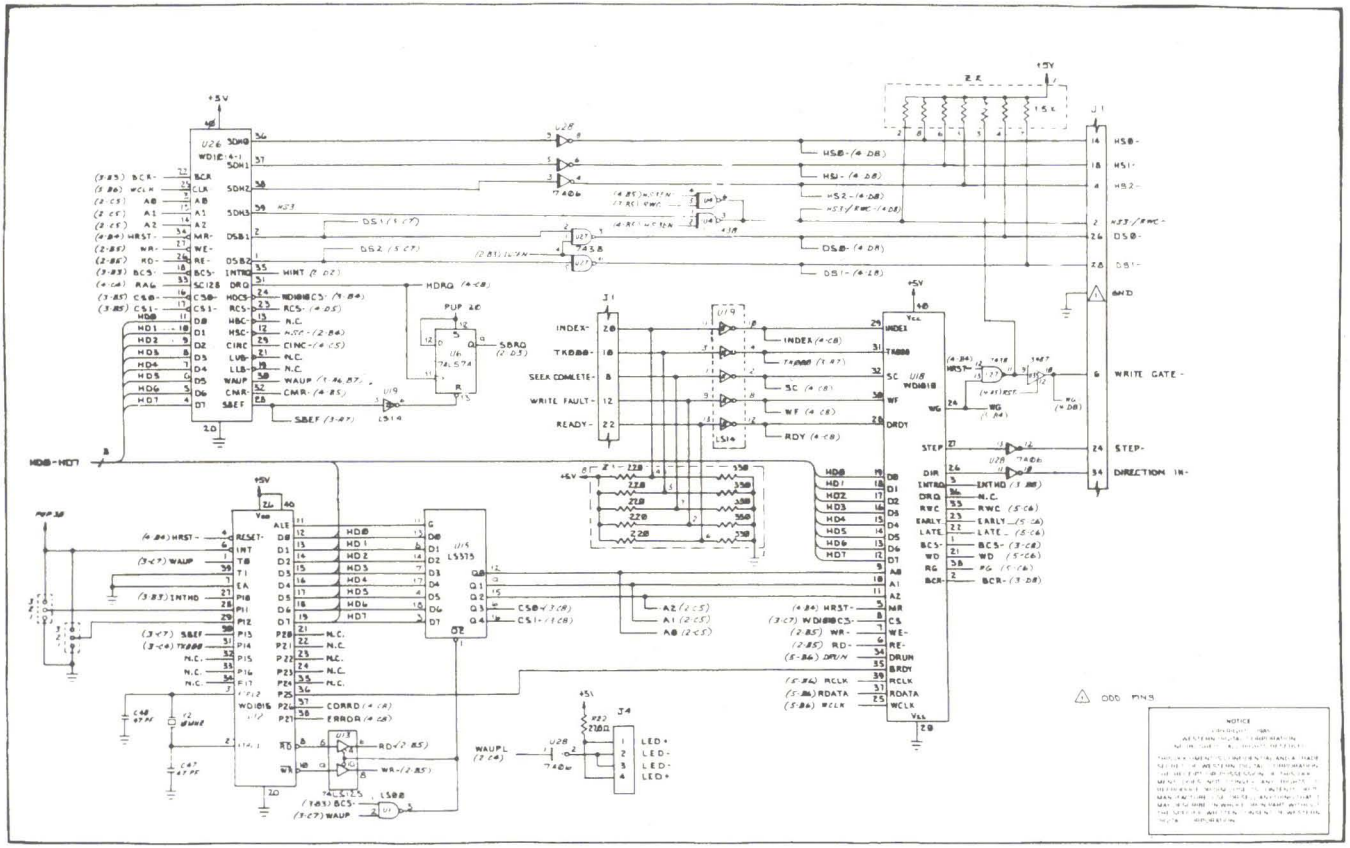


Figure 6-5. Fixed Disk Drive Controller Board Schematics (Page 3 of 5)

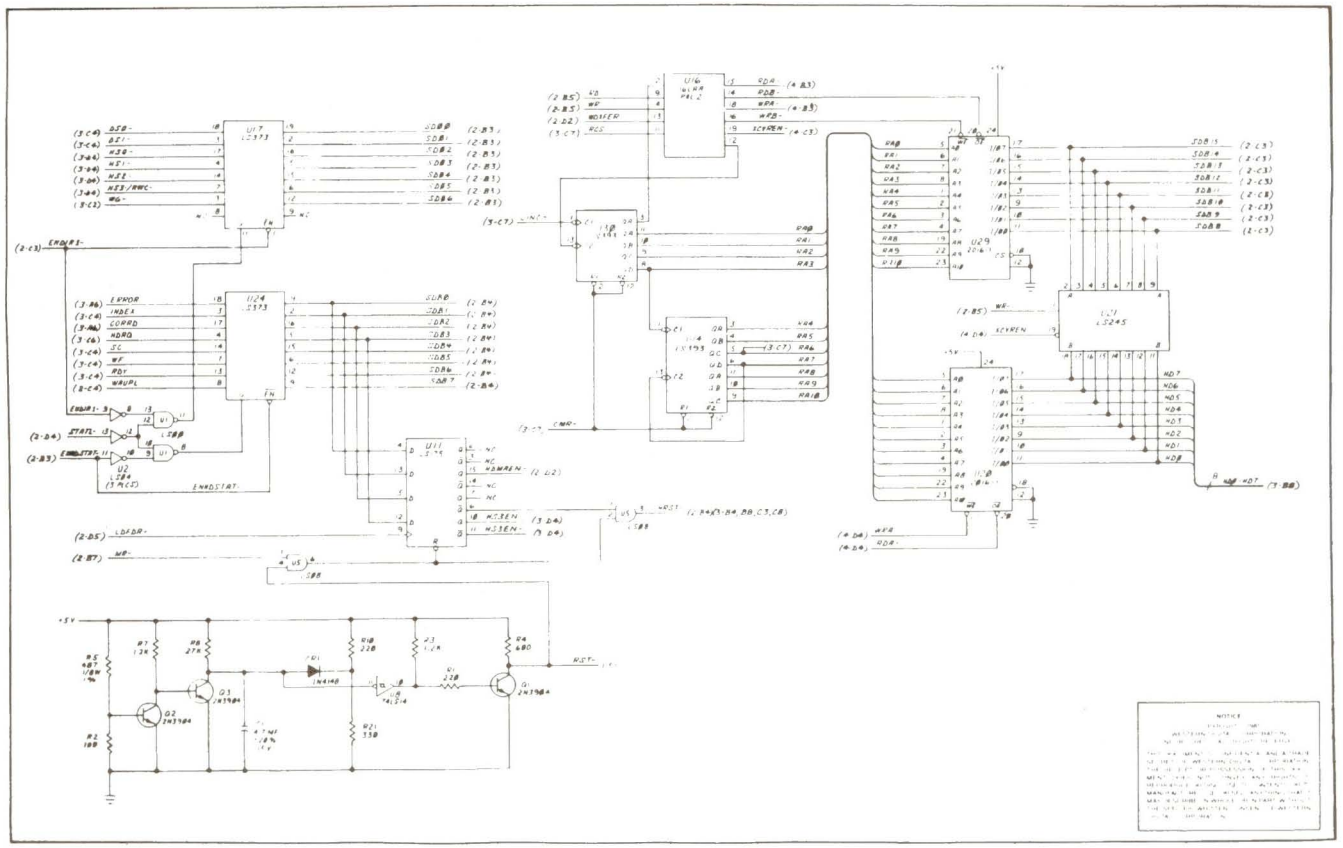


Figure 6-5. Fixed Disk Drive Controller Board Schematics (Page 4 of 5)

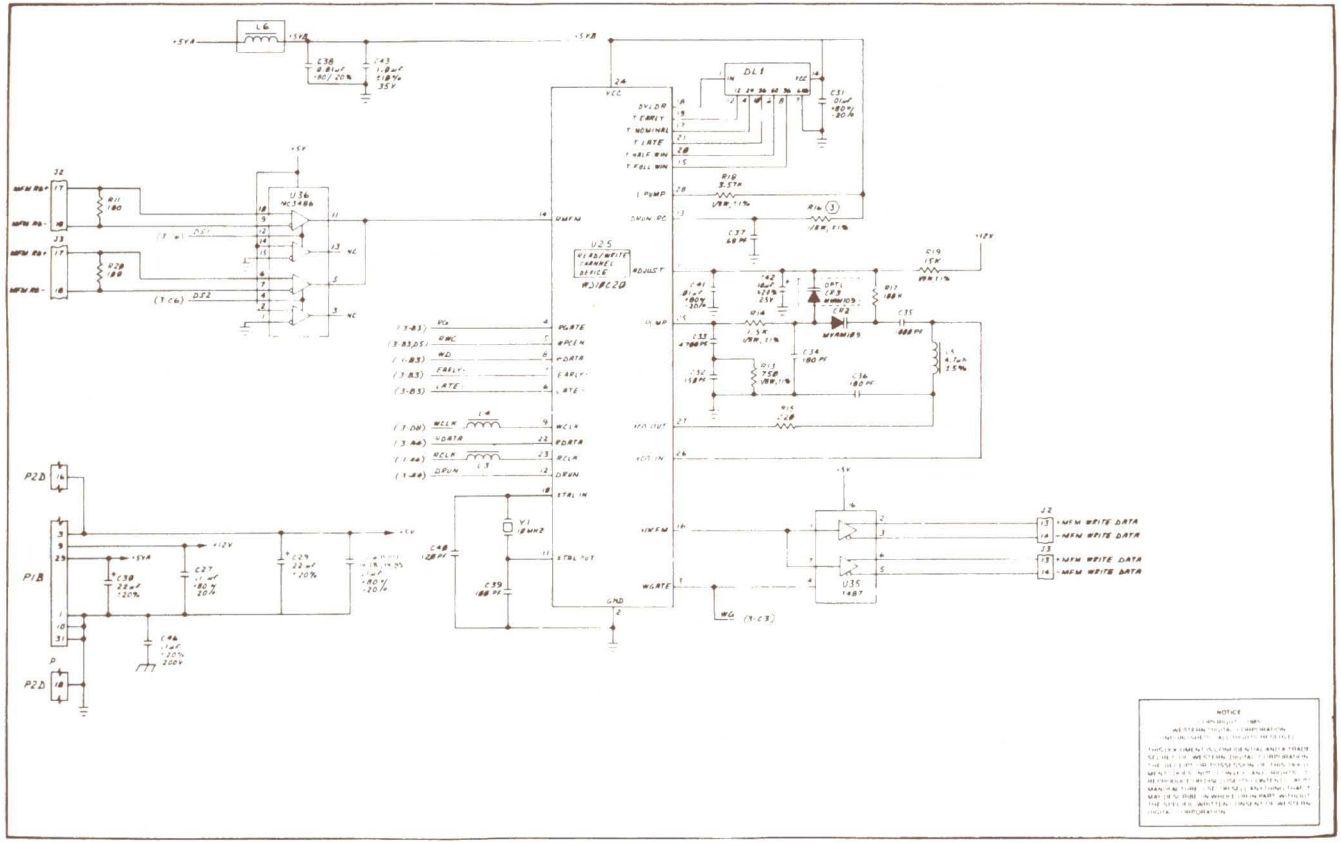


Figure 6-5. Fixed Disk Drive Controller Board Schematics (Page 5 of 5)

INDEX

INDEX

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